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Design of true-bridgeless power factor correction converter and analysing dynamic response using predictive current control with pulse train strategy

Gerçek-köprüsüz güç katsayısı düzeltmeli dönüştürücünün tasarımı ve tahmini akım kontrol yöntemi ile darbe dizisi stratejisi kullanılarak dinamik cevabının analizi

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Abstract

In this study, the design guideline for the power stage of true-bridgeless AC-DC power factor corrector (PFC) converter is provided, and working principle is explained. The dynamic responses, total harmonic distortion and power factor of true-bridgeless PFC converter are analyzed using predictive current control with pulse train strategy techniques and average current mode control for different load conditions. The main mathematical framework of the control algorithm is introduced, simulation and control charts are presented. The simulations are performed to illustrate the advantages of the method and compare it with average current mode control approach. According to the simulation results, input current complies with the IEC61000-3-2 Standards. In the control of the converter using the predictive current control with the pulse train strategy, it is observed that dynamic response of the converter is improved compared to average current control method.

Keywords: PFC, Bridgeless, Control.

Öz

Bu çalışmada, gerçek köprüsüz AC-DC güç faktörü düzeltmeli (GFD) dönüştürücünün, güç devresi tasarımı ve çalışma prensibi açıklanmıştır. Gerçek köprüsüz GFD dönüştürücünün dinamik cevabı, toplam harmonik bozulması ve güç faktörü, farklı yük koşulları için tahmini akım kontrol ile darbe dizisi stratejisi ve ortalama akım modu kontrolü teknikleri kullanılarak analiz edilmiştir. Kontrol algoritmasının matematiksel modeli tanıtılmış, kontrol şemaları ve simülasyonlar MATLAB/Simulink programı ile gerçekleştirilerek sunulmuştur. Simülasyonlar, yöntemin avantajlarını göstermek ve ortalama akım modu kontrol yaklaşımı ile karşılaştırmak için gerçekleştirilmiştir. Simülasyon sonuçlarına göre, giriş akımı toplam harmonik bozulma değerleri IEC61000-3-2 Standartlarına uygun olduğu gözükmektedir. Tahmini akım kontrolü ile darbe dizisi stratejisi kullanılarak dönüştürücünün kontrolünde, ortalama akım kontrol yöntemine kıyasla dönüştürücünün dinamik tepkisinin iyileştirildiği gözlemlenmiştir.

Anahtar kelimeler: GFD, Köprüsüz, Kontrol.

1 Introduction

With the development of technology, electronic devices have become a part of life. Therefore, efficient use of energy is essential today. Most of the devices, such as laptop chargers, LED drivers, cell phone adaptors, etc, used in daily life are powered by a DC supply. To obtain a constant DC output voltage from an AC input voltage, switching power converters are widely applied by higher requirements of its control system. Under the wide load variations and system parameter variations, they exhibit various complex dynamic behaviors [1]. The main sources of pollution in power systems and important factors for safe grid operation are non-linear loads connected to the grid. High harmonic content of input current causes effective value of input current to increase undesirably, limiting power transferred to load, deteriorating line voltage, and causing system instability. Power factor correction (PFC) circuits, which enhance power factor and decrease line current distortions, are an essential part of grid-connected AC-DC converters [2]-[7]. International standards like EN 61000-3-2 have been established to restrict harmonic values of the input current from devices connected to the network, aiming to minimize the negative impacts of these devices on the network [8]. Also, lower system costs, better dynamic response, increased efficiency by reducing losses, high power quality with low total harmonic distortion, uncomplex control capability, and higher power density are always desirable features for power converters [9]. The most common PFC method for the conventional two-stage PFC converters is the boost converter with front-end full-bridge rectifiers. To enhance efficiency of PFC converter, there is a preference for single-stage bridgeless PFC converter. This converter removes diode rectifier bridge found in conventional PFC converters and directly regulates the output voltage [10]. Several bridgeless PFC converter circuits have been designed using different control methods to correct the power factor. Such as average current mode control [11]-[15], predictive current control [16]-[19] and peak current mode control [20]. In conventional control methods (such as average current control, predictive current control [21]), the output voltage compensator and the input current current current control loop are connected in series with each other in Figure 11 and Figure 14. The input current reference peak value to be used in the current control loop is generated by the output voltage compensator. The output voltage ripple frequency (100 Hz) of AC/DC PFC converters is twice the input voltage frequency (50 Hz). For this reason, the bandwidth of the output

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voltage compensator is kept low (20 Hz) so that the change of the control signal produced by the voltage compensator is compatible with the input current frequency. If the bandwidth of the voltage compensator is increased to improve the dynamic response of the converter, the total harmonic distortion value of the input current will increase. Pulse Train strategy is a method generally used in DC-DC Boost converters to improve the dynamic response of the converter in CCM and DCM mode [22],[23]. In the proposed method in Figure 15, since the output voltage compensator is removed and the input current reference peak value is obtained from the output power, the current and voltage loops are separated from each other. For this reason, it is not possible for the loops to affect each other and the bandwidths do not slow down the dynamic response of the converter. The proposed method therefore improves the dynamic response of the converter. Metric values are given in section 6.

In this article, a new bridgeless PFC converter which has the same characteristics as the conventional boost converter is presented. Its topology is based on the modified boost converter, which has a resonant branch. Output voltage remains positive for either polarity of the input voltage. The DC conversion ratio is irrelevant to switching frequency, resonant branch parameters, and other circuit parameters. It is only related to switching duty cycle [24],[25]. The control performance of digital average current control and digital predictive current control with pulse train strategy are investigated for true-bridgeless AC/DC PFC converter. The main contribution of this article, regulation capability of mentioned control routines for the true-bridgeless AC/DC PFC converter, is explored. Comparison results are reported to present superiority of two different current control strategies. True-bridgeless AC/DC PFC converter is selected as a case study, and the closed-loop effectiveness of the two different control methods is tested using simulation tools.

In this study, it is aimed to improve the power quality by removing the full bridge at the input of a conventional full bridge step-up type AC/DC PFC converter and to improve the dynamic response of the converter with the proposed control method. In bridgeless converters, since the full bridge rectifier at the input of the conventional type converters is removed, two separate controlled switches are usually used in positive and negative half-cycle. Although the power circuit topology of the preferred converter contains two controlled switches, it provides ease of control since a single control signal is used for each semiconductor switch. This bridgeless converter is preferred because of its ease of control. The paper's structure is organized as follows: Section 2 explains design of true-bridgeless PFC converter. Section 3 ensures true-bridgeless pfc converter operating modes and mathematical verification of output voltage. Section 4 is design procedure of digital average current mode control technique. Section 5 explains digital predictive current mode control with pulse train strategy method. Section 6 presents the simulation results and comparisons of Total Harmonic Distortion (THD) and dynamic responses. Section 7 is the conclusion part of the paper.

2 Design of true-bridgeless power factor correction converter

The True Bridgeless Single Stage PFC Converter based on modified boost converter was introduced in 2010 [26] and presented in Figure 1.

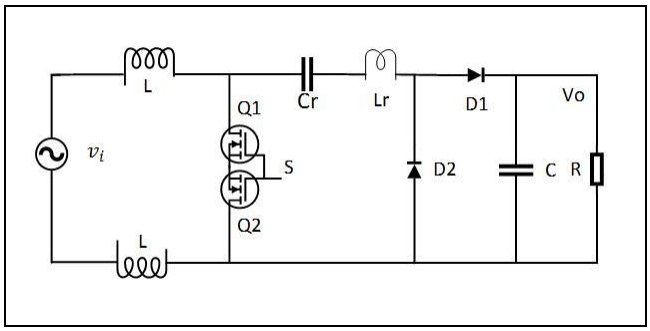

Figure 1. Circuit diagram of True-Bridgeless Single Stage PFC Converter.

Different from the traditional boost converter with front-end full-bridge rectifiers, the proposed topology eliminates front-end full-bridge rectifier and is connected a resonant branch [24]. The formula (1) which is obtained from the inductance voltage-second balance, can be used to find the inductance value. The operation of the continuous conduction mode (CCM) is ensured by the selection of the inductance value that follows.

$$L = \frac{V_g}{2\Delta i_L} DT_s \tag{1}$$

While it is generally assumed that the output power of the true-bridgeless PFC converter remains constant, minor fluctuations can occur in practice. These fluctuations are usually negligible. Unlike the output power, the input power varies continuously over time. To maintain power balance between the input stage and the load stage, the output capacitance should be chosen appropriately. The required value of the output capacitance can be determined using the following equation(2) [27] .

$$C = \frac{P_{load}}{2\omega V(\Delta V)} \tag{2}$$

Current and voltage variation on the resonant elements of true bridgeless pfc converter during operation is shown in Figure 2.

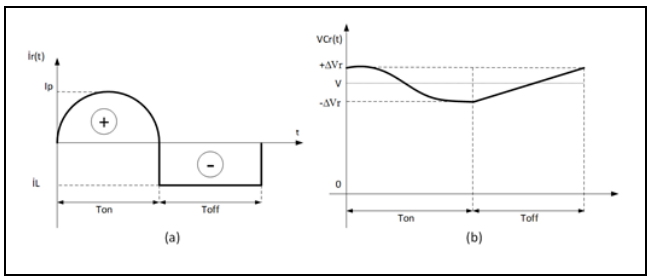

Figure 2. The negative half cycle condition (a): Resonant inductance current waveform. (b): Resonant capacitor voltage waveform.

To determine optimal value of resonant branch elements, some criteria should be considered. The switching strategy of the topology is constant switching frequency(CF) operation and constant on-time(CO) operation. In the operation where the switching frequency is kept constant, the conduction time of the controlled switch varies depending on the duty cycle. Conversely, in the operation where the conduction time of the controlled switch is kept constant, the switching frequency changes. When the true-bridgeless pfc converter works in CF-operation mode, a coasting zero current interval occurs is shown in Figure 3. To eliminate the coasting zero current interval for higher efficiency, CO-operation mode should be

used. However, CO-operation increases the main inductance value. In summary, CF-operation mode is more suitable than CO-operation mode [28].

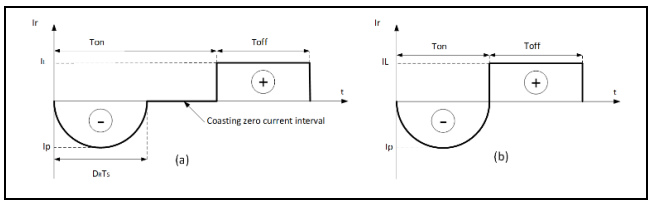

Figure 3. Resonant inductance current waveform. (a): Constant switching frequency resulting in a coasting zero current interval. (b): Constant ON-time eliminates zero current coasting interval.

To increase efficiency in CF-operation mode, half cycle of resonance period T_r should be completed within the ON-time of the switching period T_s. Consequently, to ensure that the ON-time of switching period above defined half cycle of resonance period(5)(6).

$$fr = \omega_r/2\pi \tag{3}$$

$$\omega_r = 1/\sqrt{L_r C_r} \tag{4}$$

$$T_{ON} = D_R T_s = {}^{T_r}/_{2} \tag{5}$$

$$D_R = {}^{f_s}/_{2f_r} \tag{6}$$

The resonant frequency f_r range, which is determined(3)(4) by the selected resonant component (L_r and C_r), is defined by conduction time of controlled switch, T_{ON}. The duty cycle is influenced by difference between output voltage V_o and peak input voltage . V_i According to equation (7), higher duty cycles are observed for lower input voltages.

$$D = 1 - \frac{V_i}{V_o} \tag{7}$$

In cases where difference between input voltage and output voltage is smaller. Resonance period decreases depending on the decrease of switching on-time period. In this case, since resonance frequency increases, the current amplitude on the resonant inductance drastically increases(8), causing an increase in current stress and conduction losses on all components. However, the voltage ripple and voltage stress on the resonant capacitor also increase(9) (10) [28].

$$I_p = I_o \frac{\pi * f_r}{2 * f_s} \tag{8}$$

R_N ,characteristic impedance (Natural Resistance)(9), i_r ,current on the resonant inductance(10), ΔVC_r voltage variation on the resonant capacitor(11).

$$R_N = \sqrt{L_r/C_r} \tag{9}$$

$$i_r = \frac{\Delta VC_r}{R_N} = \Delta VC_r * \sqrt{\frac{C_r}{L_r}} = \frac{\pi * P_{out}}{V_{out} - V_{in}} \tag{10}$$

$$\Delta VC_r = \frac{\pi * P_{out}}{V_{out} - V_{in}} * \sqrt{\frac{L_r}{C_r}} \tag{11}$$

To keep the resonance frequency at the same value, resonant capacitor would be low value and resonant inductance would be high value. In order to reduce voltage stresses and semiconductor losses, the value of the resonance inductance should be very small ($L_r \ll L$) compared to the value of the pwm(main) inductance. The decrease in the value of the resonant capacitor causes higher voltage ripple and voltage stress on itself and the controlled semiconductor components. However, decreasing the resonant capacitance C_r causes increased voltage ripple V_{c_r} which leads higher voltage stress at the resonant capacitor and controlled switch(11). In practice, resonant capacitor type can be defined according to maximum allowed voltage ripple on itself. In order to tolerate larger voltage ripples, multiple capacitors can be connected in series.

However, if the output voltage increases, high-value resonance elements are needed. The increase in the value of the resonant inductance leads to higher conduction resistance and consequently, an increase in losses. This results in worse switching behaviour. Additionally, stronger insulation is required for passive components.

The resonant frequency determines the sizing of the resonant elements, L_r and C_r. While these elements do not directly impact the amplitude of the resonant current, their ratio, L_r/C_r, must be carefully chosen to ensure optimal system performance. This selection aims to minimize component stress and overall system losses, leading to efficient operation [9].

As shown in Figure 4, as long as the resonance frequency is constant, changing the L_r value does not affect the peak value of the resonance current. As long as the load current is constant, the peak value of the resonance current changes in direct proportion to the resonance frequency.

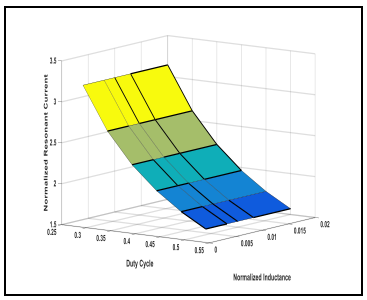

Figure 4. Resonance inductance peak current amplitude variation.

According to Figure 5, when the resonance frequency is constant, the voltage fluctuation on the resonance capacitor will increase as the increase in the value of the resonance inductance will cause the value of the resonance capacitor to decrease.

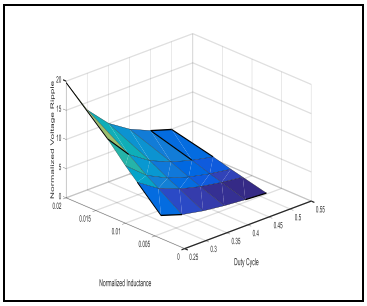

Figure 5. Resonant capacitor voltage ripple.

L_r and $C_r$values can be in different combinations. The choice made affects the current stress on the $L_r$component and the voltage stress on the C_r component. For this reason, it should be designed in such a way that the voltage and current stresses are at the lowest level as a simulation, not as an equation. There are two factors that determine the current stress on the inductance L_r. In Equation 8, since the switching frequency is constant, these parameters are the resonant frequency and the output current and therefore the output power. The voltage stress on the C_r component increases with the increase of the output power. Figure 6 shows that the current stress on the $L_r$component and the voltage stress on the C_r component increase with the output power change.

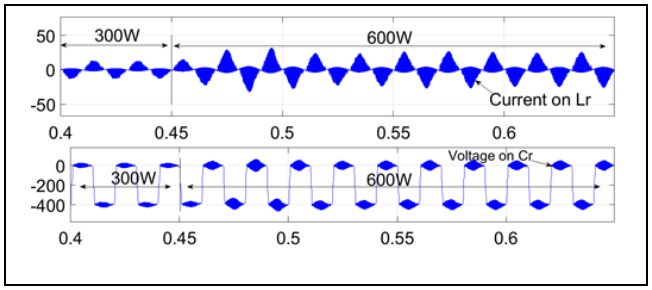

Figure 6. Current on $L_r$and voltage on C_r for step load 300W to 600W.

When the output power is constant, the factor determining the current stress on the L_r component is the resonance period. The voltage stress on the C_r component is the value of the L_r component according to Figure 5. According to Equation 5, the parameter that determines the resonance period will be the duty cycle. According to Equation 7, the duty cycle will be 0.22 for input voltage 220V and output voltage 400V. In this case, L_r =5.5µs. The voltage on C_r for L_r =1.32 µH and C_r =580nF is given in Figure 7. The voltage on C_r for L_r = 13.2µH and C_r =58nF is given in Figure 8. When the simulation results are analysed, the voltage stress on the resonant capacitor increases as its value decreases. In this context, the L_r value should be as small as possible and the C_r value should be as large as possible.

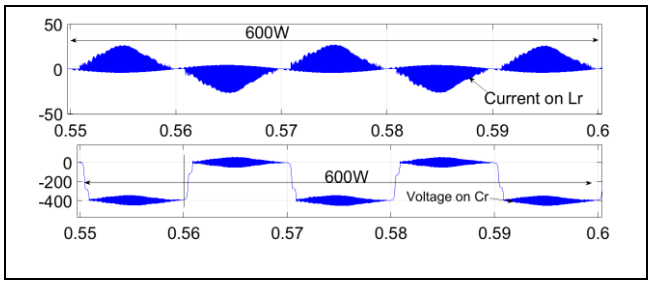

Figure 7. Current on L_r and voltage on C_r at 600W for L_r =1.32µH and C_r =580nF..

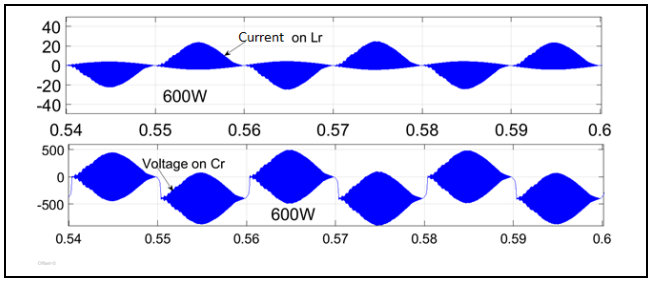

Figure 8. Current on L_r and voltage on C_r at 600W for L_r =13.2µH and C_r =58nF .

3 True-bridgeless power factor correction converter operating modes and analysis of output voltage

3.1 Positive half cycle working states

There are two different conditions for switches in positive half cycle of line voltage. When controlled semiconductor switch is on, diode D2 is turned on and diode D1 is turned off. When the controlled semiconductor switch is off, D1 is on and D2 is off. Positive half cycle working states are shown in the Figure 9.

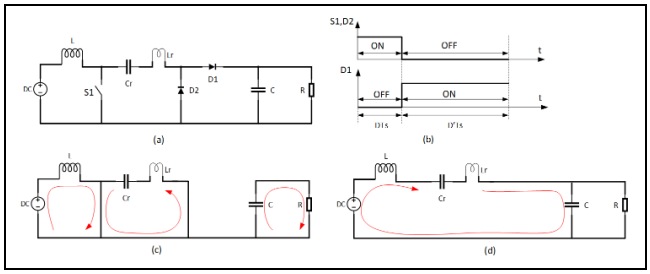

Figure 9(a): True-Bridgeless AC/DC PFC converter.
(b): Switches on-off state for positive half-cycle.
(c): Controlled switches on state for positive half-cycle.
(d): Controlled switches off state for positive half-cycle.

V_i, input voltage, D, duty cycl, V_o, output voltage. According to inductor volt-second balance can be written as follow;

$$V_i DT_s + (V_i - V_o - VC_r)(1-D)T_s = 0 \quad (12)$$

While

$$VC_r = 0 \quad (13)$$

$$V_i DT_s = (V_o + VC_r - V_i)(1-D)T_s \quad (14)$$

$$V_o = \frac{1}{(1-D)} * V_i \quad (15)$$

3.2 Negative half cycle working states

There are two different conditions for switches in negative half cycle of line voltage. When the controlled semiconductor switch is on, diode D1 is on and diode D2 is off. When controlled semiconductor switch is off, D1 is off and D2 is on. Negative half cycle working states are shown in the Figure 10.

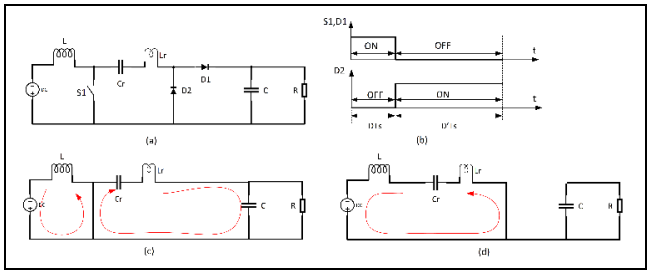

Figure 10. Negative half cycle working states.
(a): True-Bridgeless AC/DC PFC converter. (b): Switches on-off state for negative half-cycle. (c): Controlled switches on state for negative half-cycle. (d): Controlled switches off state for negative half-cycle.

$$V_i DT_s + (V_i - VC_r)(1-D)T_s = 0 \quad (16)$$

While

$$VC_r = V_o \tag{17}$$

$$V_i D T_s = (V_o - V_i)(1 - D)T_s \tag{18}$$

$$V_o = \frac{1}{(1-D)} * V_i \tag{19}$$

4 Digital average current control for true-bridgeless power factor correction converter

The average current mode(ACM) control method is one of the power factor correction methods widely used in AC/DC converters [29] - [31]. The Digital ACM-controlled true-bridgeless AC/DC PFC converter's block diagram is shown in Figure 11.

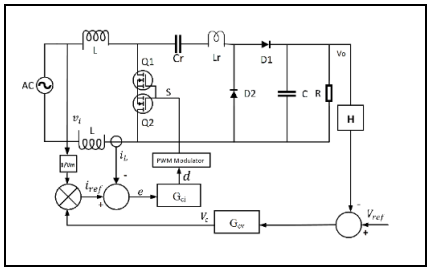

Figure 11. Block diagram of the digital ACM-controlled true-bridgeless PFC converter.

G_{ci} is the transfer function of the inner loop compensator, G_{cm} is gain of current compensator, ω_{zi} is the zero of the current compensator, ω_{pi} is pole of the current compensator. V_i is input voltage, V_o is output voltage, e_i is current error, e_v is output voltage error, V_c is output of voltage compensator, d is duty cycle of pwm signal controlling main switch. G_{cv} is transfer function of the voltage compensator, G_{vm} is the gain of the voltage compensator, ω_{zv} is the zero of the voltage compensator.

$$G_{ci}(s) = G_{cm}\frac{1 + \frac{\omega_{zi}}{s}}{1 + \frac{s}{\omega_{pi}}} \tag{20}$$

For digital implementation, the equation of the current compensator given is as

$$\begin{aligned} d(n) = d(n-1)\frac{8}{2\omega_{pi}T_s + 4} + d(n-2)\frac{2\omega_{pi}T_s - 4}{2\omega_{pi}T_s + 4} + \\ e_i(n)\frac{G_{cm}\omega_{pi}T_s(\omega_{zi}T_s + 2)}{2\omega_{pi}T_s + 4} + \\ e_i(n-1)\frac{2G_{cm}\omega_{pi}(\omega_{zi}{T_s}^2)}{2\omega_{pi}T_s + 4} + \\ e_i(n-2)\frac{G_{cm}\omega_{pi}T_s(\omega_{zi}T_s - 2)}{2\omega_{pi}T_s + 4} \end{aligned} \tag{21}$$

Figure 12 shows the bode curve of compensated inner loop of the Digital ACM-controlled True-Bridgeless PFC Converter.

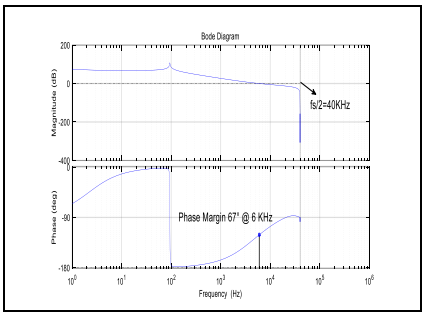

Figure 12. Bode plot for compensated inner loop of the Digital ACM-controlled True-Bridgeless PFC Converter.

The inner loop function needs to be designed in a manner that ensures a first-order response devoid of oscillations, the loop function is characterized by a -20 dB/decade slope and maintains a phase angle of around 67 degrees at crossover frequency, which is established at 6 KHz. to attenuate switching ripples and their harmonics sufficiently. To ensure the desired phase angle and crossover frequency, the current compensator ω_{zi} zero must be located at low frequency region and current compensator pole ω_{pi} must be located at high frequency region.

$f_{zi} = 2\ KHz,\ f_{pi} = 20\ KHz, G_{cm} = 0.63$

The transfer function of the voltage compansator

$$G_{cv}(s) = K_p + \frac{K_i}{s} \tag{22}$$

G_{cv} is the transfer function of PI controller. In DSP microcontroller applications, if transfer function in s domain is discretized with respect to the z domain; it is expressed as follows:

$$\begin{aligned} V_c(n) = V_c(n-1) + K_p\big(e_v(n) - e_v(n-1)\big) \\ + \frac{K_i T_s}{2}(e_v(n) + e_v(n-1)) \end{aligned} \tag{23}$$

The bode curve for compensated outer loop of the Digital ACM-controlled True-Bridgeless PFC Converter shown in Figure 13. Voltage compensator is adjusted to regulate output voltage to desired value. At the same time output of outer loop compensator produces peak value of input current reference. Voltage loop is configured with a significantly low bandwidth to ensure that fluctuations in the output voltage do not affect the generated reference current. In order for the voltage compensator not to detect fluctuation occurring in the output voltage, the bandwidth must be kept below 100 Hz [27]. $K_p = 0.83$, $K_i = 176$.

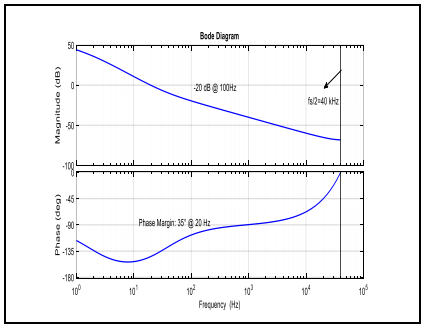

Figure 13. Bode plot for voltage compansator bandwith at 20 Hz of the Digital ACM-controlled True-Bridgeless PFC Converter.

5 Digital predictive current control with pulse train strategy for true-bridgeless power factor correction converter

The major difference of the proposed control method from the predictive current control method [21] is that the voltage and current loops are separated from each other. For this reason, it was explained in the introduction that the voltage control loop does not affect the current control loop. Figure 14 shows the schematic of the predictive current control method.

Digital predictive current mode control with pulse train strategy true-bridgeless AC/DC PFC converter's block diagram is shown in Figure 15. In predictive current mode control, the measured output voltage is compared with desired reference value of the output voltage. Then, output voltage error is used by PI controller like average current mode control. Output data of G_{cv}, that is PI controller, V_c (peak value of the reference current) is multiplied with a gain to produce inductor current reference.

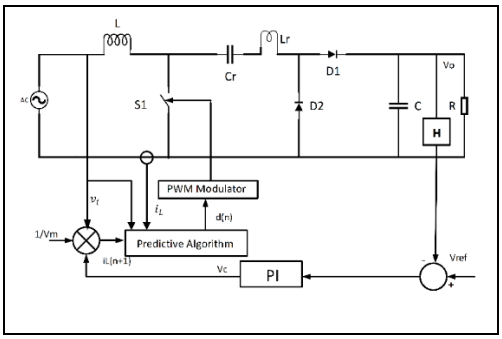

Figure 14. Predictive current mode control schematic for true-bridgeless PFC converter.

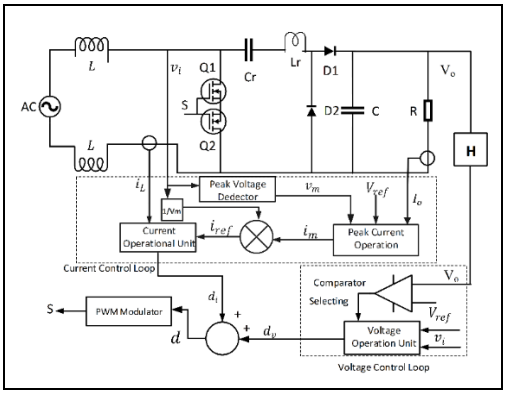

Figure 15. Block diagram of digital predictive current mode control with pulse train strategy true-bridgeless PFC converter.

The gain is normalized value of input voltage. The produced current reference and the measured input current are used by the predictive controller to calculate the desired duty cycle. In the last step, the linear modulator produces the gate pulse. The central concept behind predictive current mode control is to enforce that average value of inductor current matches reference inductor current [32],[33]. Discrete-time model of inductor current is given by

$$I_L(n+1) - I_L(n) = \frac{V_i(n)T_s}{L} - \frac{\big(1-d(n)\big)V_o(n)T_s}{L} \qquad (24)$$

According to (24), the inductor predicted current $I_L(n+1)$ can be produced by output voltage V_o, the measured inductor current $I_L(n)$ and input voltage V_i. By solving (24) for duty cycle d(n), the following expression is obtained.

$$d(n) = \frac{L}{T_s}\frac{I_L(n+1) - I_L(n)}{V_o(n)} + \frac{V_o(n) - V_i(n)}{V_o(n)} \qquad (25)$$

The reference output voltage can be plugged into (25) for the variable V_o, and the results

$$d(n) = \frac{L}{T_s}\frac{I_L(n+1) - I_L(n)}{V_{ref}(n)} + \frac{V_{ref}(n) - V_i(n)}{V_{ref}(n)} \qquad (26)$$

The detailed derivation of (24) can be found in [21]. The instantaneous reference current is expressed as

$$I_L(n+1) = I_{peak} * |sin\ \omega t(n+1)| \qquad (27)$$

In (27), I_{peak} refers to the peak value of the reference current.

In digital predictive current mode control with pulse train strategy method, to attain both unity power factor (PF) and a rapid dynamic response, the output voltage control loop and the inductor current control loop are separated.

To adjust the output voltage, the output voltage is compared with the reference voltage after each sampling to obtain the duty cycle according to the open-loop voltage transfer function of the bridgeless boost type AC/DC converter(28).

$$D = \frac{V_{ref}(n) - V_i(n)}{V_{ref}(n)} \qquad (28)$$

In pulse train strategy, the inductor current peak value i_m is obtained from equation (29), which can be written by benefiting input-output power equality under 100% efficiency assumption. This equation requires additional current measurement of load current. Amplitude of inductor current i_m is produced by output power.

$$i_m = \frac{2P_o}{V_m} = \frac{2V_oI_o}{V_m} \qquad (29)$$

Inductor reference current i_{ref} is optained by multiplying peak value of input current $i_m$with input voltage V_i, i_{ref} is given as

$$i_{ref}(n) = i_L(n+1) = \frac{2V_iV_{ref}I_o}{{V_m}^2} \qquad (30)$$

Where V_i is ac input voltage,

$$V_i = \sqrt{2}V_s\, sin(\omega t) \qquad (31)$$

V_s is rms value of input voltage, V_{ref} is output voltage referance. Peak voltage detector determines amplitude of input voltage V_m. The current duty cycle d_i is generated using the predictive current control algorithm for power factor correction of input current with respect to the reference current.

$$d_i = \frac{L}{T_s}\frac{i_{ref}(n) - I_L(n)}{V_{ref}(n)} \qquad (32)$$

In this control method, since the PI controller used for output voltage regulation is eliminated, output voltage regulation must be performed using the pulse train strategy [22], [34], [35].

Therefore, voltage regulation duty cycle d_v is generated for output voltage regulation is as shown in equation;

$$d_v = K * D = K * \frac{V_{ref}(n) - V_i(n)}{V_{ref}(n)} \quad (33)$$

Duty cycle generated for both output voltage regulation and input current power factor correction is given as equation;

$$d(n) = d_v + d_i \quad (34)$$

$$d(n) = K * \frac{V_{ref}(n) - V_i(n)}{V_{ref}(n)} + \frac{L}{T_s}\frac{i_{ref}(n) - I_L(n)}{V_{ref}(n)} \quad (35)$$

Here, K coefficient is derived based on the converter input voltage and output reference voltage. Two different values of the K coefficient are generated, the highest value K_H and the lowest value K_L.

$$K = 1 + \frac{2\omega L V_{ref}^2}{R V_m (V_{ref} - V_i)} cos\,(\omega t) \quad (36)$$

Variation of K_{max} and K_{min} coefficient with respect to the input and output reference voltage are given in Figure 16 and Figure 17 respetively. Here the grid frequency ω, input inductance L value and output load R are constant. The variation of the K coefficient over half-line period is shown in Figure 18. For output voltage regulation, duty cycle value is calculated by sampling output voltage. If the output voltage value is lower than the reference value, the high value coefficient K_H is applied, if the output voltage value is higher than the reference voltage value, the low value coefficient K_L is selected [36], [37].

$$K = \begin{Bmatrix} K_H\,, V_o \le V_{ref} \\ K_L,\ \ V_o > V_{ref} \end{Bmatrix} \quad (37)$$

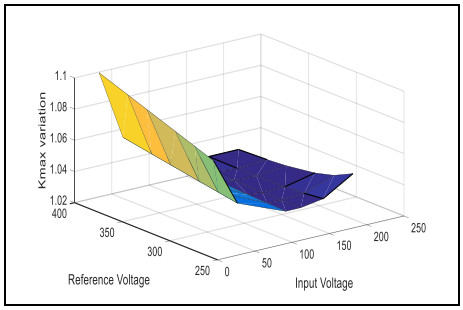

Figure 16. Variation of K_{max} coefficient with respect to the input and output reference voltage.

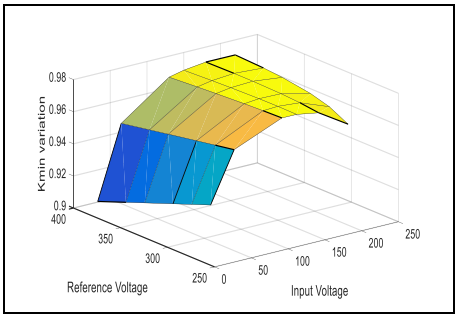

Figure 17. Variation of K_{min} coefficient with respect to the input and output reference voltage.

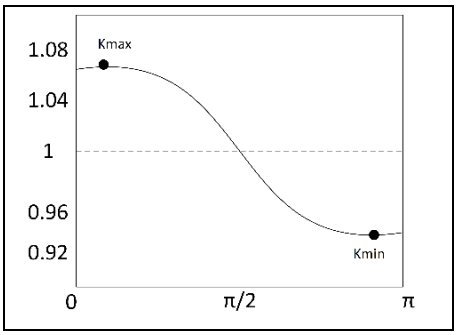

Figure 18. K over half-line period.

6 Simulation results

The simulations of the converter were done using the Matlab / Simulink program. Simulink model is given in Figure 19. Since Simulink MATLAB Function block is used for the simulation, the control method is performed in discrete time. For this reason, the compensator discrete-time equations given in the article can be used in microcontrollers such as DSP530F28335. Frequency response method approach and continuous-time to discrete-time bilinear mapping technique are used to set the parameters of the discrete-time equations of the controllers to be used by the DSP microcontroller. Dynamic response of system to load change and total harmonic distortion rates will be compared using the true-bridgeless converter, average current control method and predictive current control with pulse train strategy. The converter will first be operated at half load (300W), then by stepping to full load (600W), a comparison will be made between the dynamic response (step response) and total harmonic distortion of converters during transition. The parameters used in the simulation is given in Table 1. According to the pulse train strategy, after each sampling signal, the code in the DSP is processed and the K value must be determined at the end of the code. In Equation 37, it is stated which K_H and K_L value will be selected under which condition.

Table 1. Simulation parameters.

Parameter	Description	Values
P_o	Output Power	600[W]
V_o	Output Voltage	400[V]
V_{in}	Input Voltage	220[V_{rms}]
f_s	Switching Frequency	80[KHz]
L_r	Resonant Inductor	1.32[µH]
C_r	Resonant Capacitor	580[nF]
C_o	Output Capatior	540[µF]
L	Inductor	4[mH]
T_s	Sampling Period	12.5[µs]

Here, the switching frequency at which the DSP will be operated is determined according to the sampling period of the DSP and therefore according to the processing time of the code in the DSP. In this application, the sampling period is determined as $T_{sample} = 12.5$ µs. Therefore, each pulse generated by the DSP to drive the controlled switches will be refreshed every 12.5 µs. For this reason, the switching frequency $f_s = 80\ KHz$ (switching frequency period $T_s = 12.5$ µs) is determined. Figure 20 and Figure 21 show the input current, total harmonic distortion and power factor values of the Bridgeless AC/DC PFC converter and conventional full bridge rectified AC/DC PFC boost converter for 600W power while using average current control, respectively.

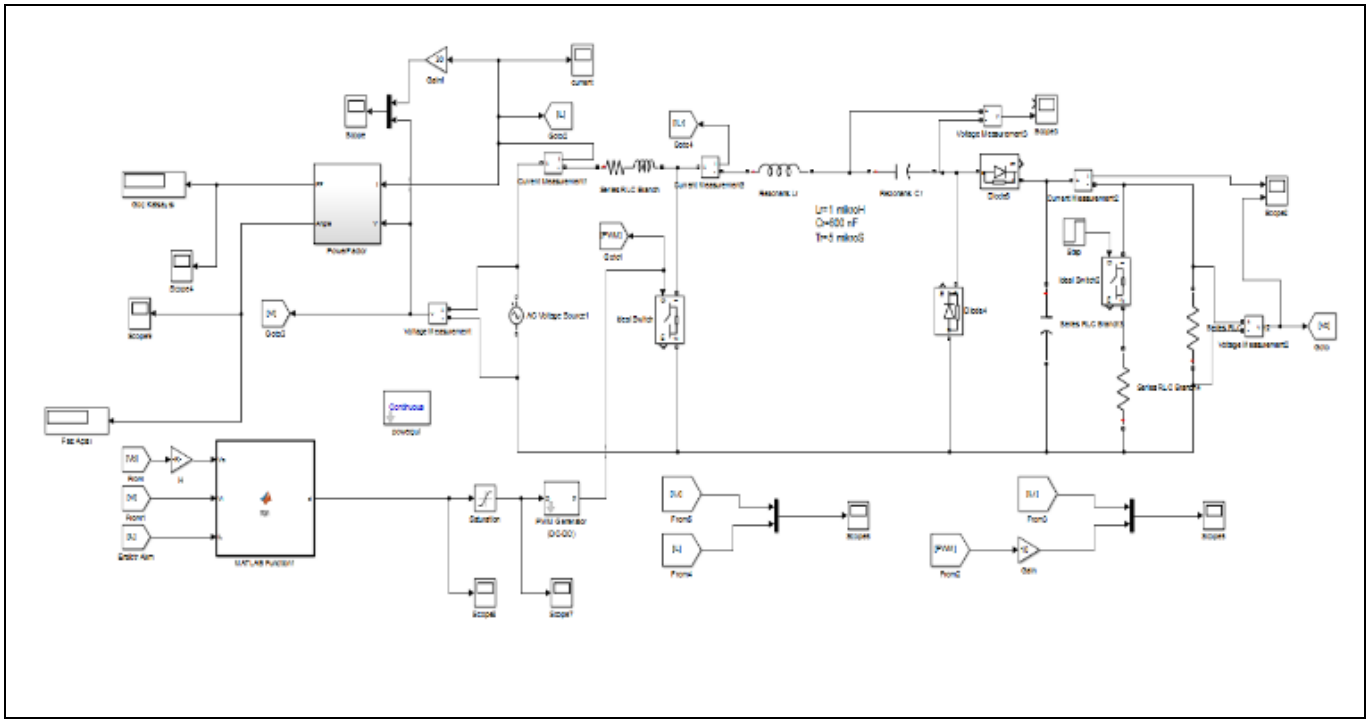

Figure 19. True-Bridgeless simulink model.

Figure 20 shows the total harmonic distortion (THD=5.84%) and power factor (PF=0.9998) of the true-bridgeless AC/DC PFC converter. In Figure 21, the total harmonic distortion value (THD=5.96%) and power factor (PF=0.994) of the conventional type AC/DC PFC Boost Converter are given. When the results are evaluated, it is seen that the power quality of the true-bridgless converter is better.

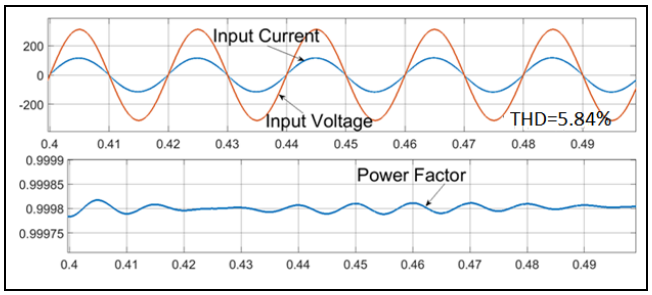

Figure 20. AC/DC PFC bridgeless converter ınput voltage, ınput current and power factor.

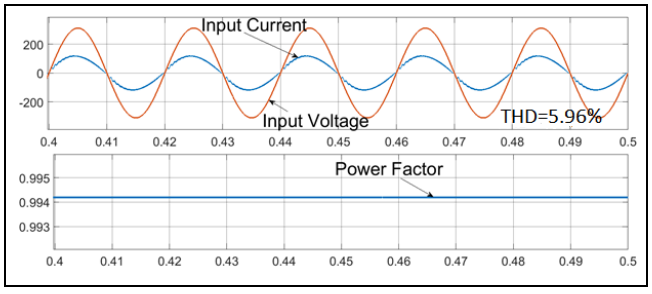

Figure 21. AC/DC pfc conventionel boost converter ınput voltage, ınput current and power factor.

For the average current control method, the bode curve for the voltage compensator bandwidth of 20 Hz is as shown in Figure 13 and simulations are performed according to 20 Hz bandwidth. Figures 22 and 23 show the input voltage, input current and output voltage waveforms of the PFC converter from half load to full load (300W to 600W) and steady state for the average current control method respectively.

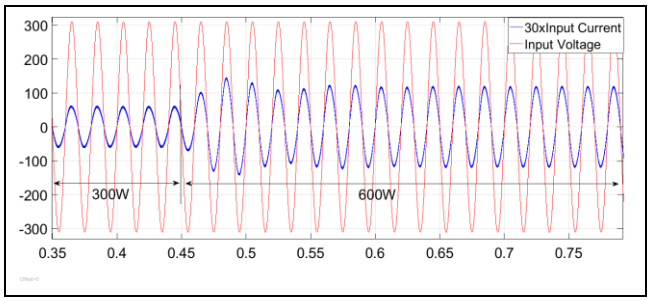

Figure 22. Input voltage and current vaweforms during transition from 300W to 600W for average current control method.

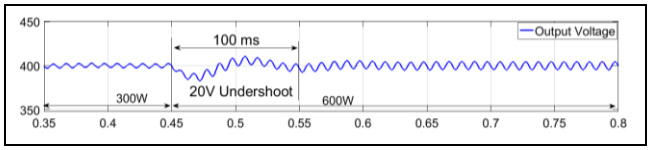

Figure 23. Dynamic response of output voltage during transition from 300W to 600W for average current control method banndwith 20 Hz.

In Figure 23, during the transition from half load to full load, the settling time of the voltage to the desired value is 100 ms and the voltage undershoot during the transition is 20V. In Figure 24 and 25, the total harmonic distortion value at 600W output power is measured as 5.84%. The output voltage compensator bandwidth 60 Hz bode plot in Figure 26, the total harmonic distortion value in Figure 27 is 8.92%, the converter

dynamic response of load step in figure 28 is 25 ms settling time and the voltage undershoot is 10V. When the bandwidth of the voltage compensator is increased, it is observed that the dynamic response of the system improves but the input current total harmonic distortion increases.

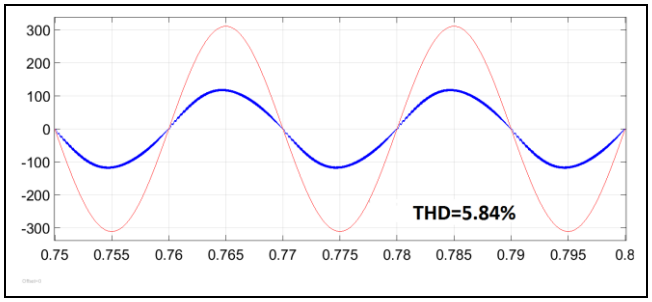

Figure 24. Input current and input voltage for average current mode control bandwith 20 Hz at 600W power.

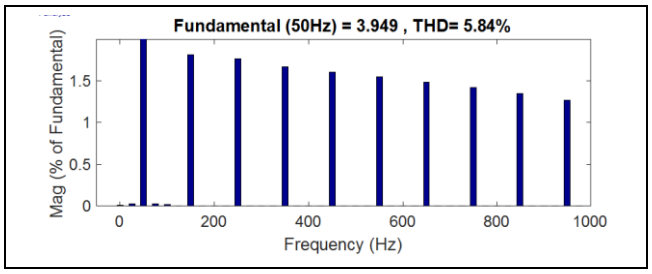

Figure 25. Total harmonic distortion (THD) of true-bridgeless converter for average current mode control.

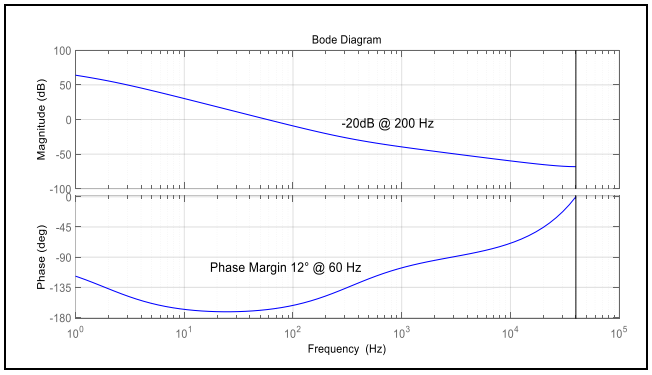

Figure 26. Bode plot for voltage compansator bandwith at 60 Hz of the Digital ACM-controlled True-Bridgeless PFC converter.

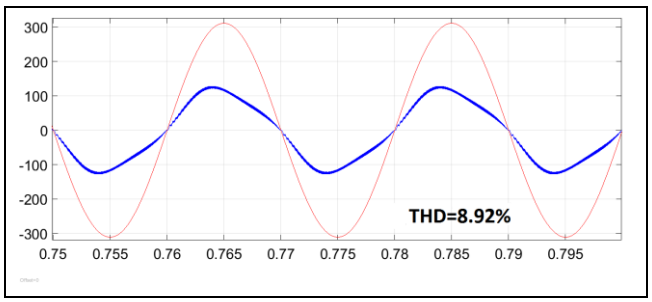

Figure 27. Input current and input voltage for average current mode control bandwith 60 Hz at 600W power.

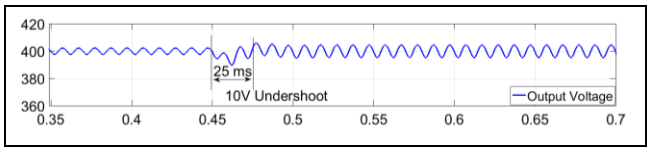

Figure 28. Dynamic response of output voltage during transition from 300W to 600W for average current control method banndwith 60 Hz.

Figures 29 and 30 show the input voltage, input current and output voltage waveforms of the PFC converter from half load to full load (300W to 600W) and steady state for the predictive current control method with pulse train strategy respectively. In Figure 30, during the transition from half load to full load, the settling time of the voltage to the desired value is 10 ms and the voltage undershoot during the transition is 5V. In Figure 31 and Figure 32, the total harmonic distortion value at 600W output power is measured as 7.25%. When the predictive current control method with pulse train stretegy is used, the dynamic response of the converter is quite good since the voltage and current loops are separate from each other. Input current and voltage waveforms for both control methods are in same phase. Thus, it results in minimal overall harmonic distortion and excellent power factor. According to the simulation results, it is seen that the converter input current total harmonic distortion values for both methods comply with the IEC61000-3-2 (Input current 3rd harmonic value must be less than 30%) standard.

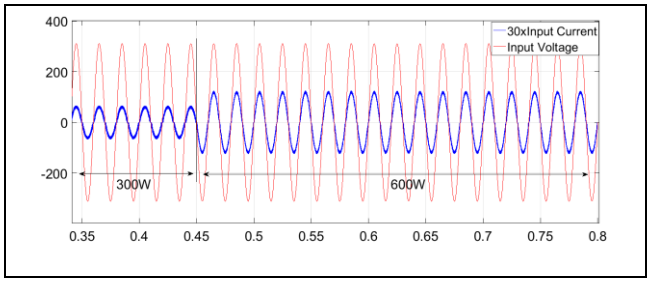

Figure 29. Input voltage and current vaweforms during transition from 300W to 600W for predictive current mode control with pulse train strategy.

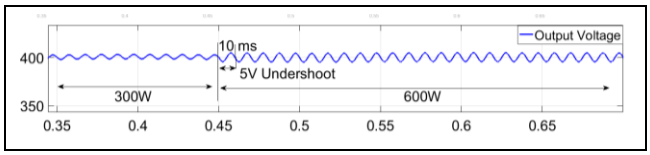

Figure 30. Dynamic response of output voltage during transition from 300W to 600W for predictive current control with pulse train strategy control.

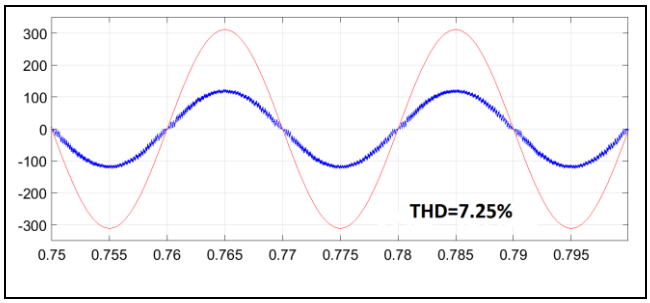

Figure 31. Input current and input voltage for predictive current control with pulse train strategy at 600W power.

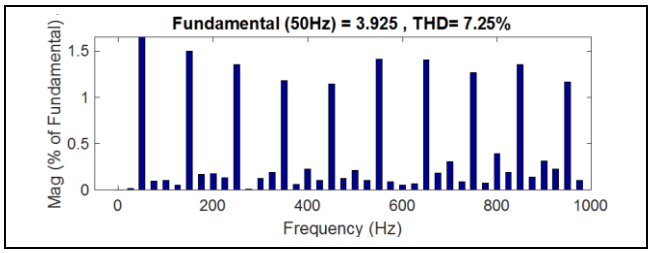

Figure 32. Total harmonic distortion (THD) of the true-bridgeless converter for purposed method.

Table 2. THD and step response results for control method.

Control Method	600W @ 50Hz Step Response	600W @ 50Hz THD%
Average Current Mode	100 ms	5.84%
Predictive Current Control with Pulse Train Strategy	10 ms	7.25%

Figure 33 shows input voltage and input current for the predictive current control. Figure 13 shows the output voltage compensator bandwidth 20 Hz bode plot, Figure 34 shows the total harmonic distortion value is 5.91%, Figure 35 shows the converter dynamic response of load step, the voltage undershoot is 25V and settling time is 200 ms. The output voltage compensator bandwidth 60 Hz bode plot in figure 26, the total harmonic distortion value in figure 36 is 9.94%, the converter dynamic response of load step in Figure 37 is 25 ms settling time and the voltage undershoot is 12V. Considering the simulation results, it is seen that when the bandwidth of the output voltage compensator is increased in the predictive current control method, the dynamic response of the converter improves, but the input current total harmonic distortion value increases and deteriorates. In the proposed method, since the output voltage compensator is eliminated and the voltage control loop is separate from the input current control loop, they do not affect each other.

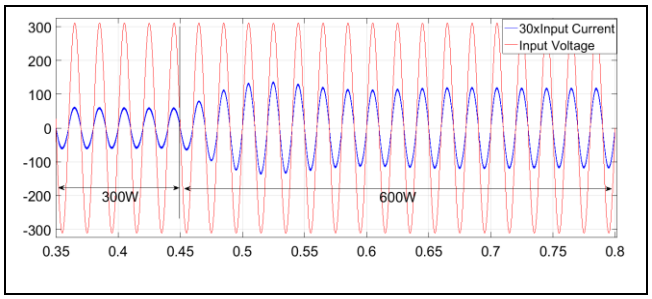

Figure 33. Input voltage and current vaweforms during transition from 300W to 600W for predictive current control.

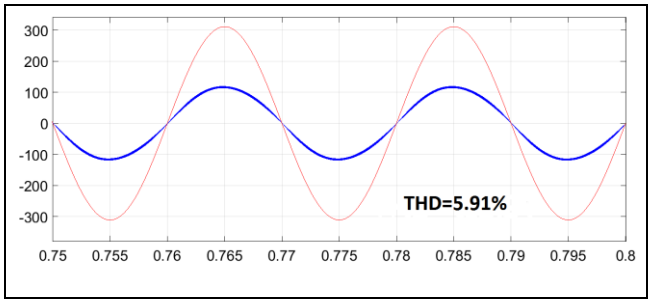

Figure 34. Input voltage and current vaweforms for predictive current control bandwith 20 Hz at 600W power.

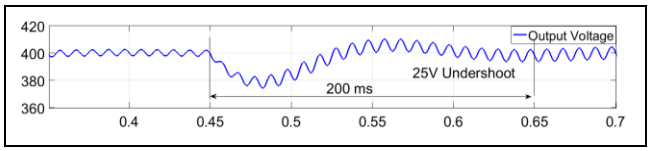

Figure 35. Dynamic response of output voltage during transition from 300W to 600W for predictive current control bandwith 20 Hz.

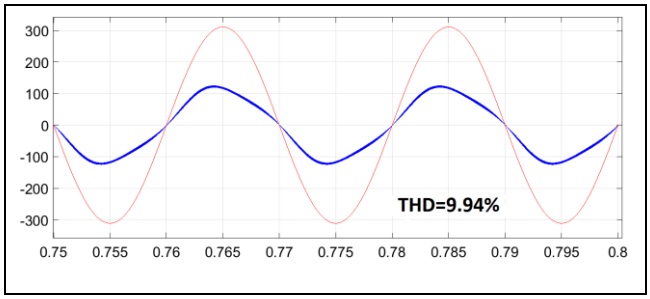

Figure 36. Input voltage and current vaweforms for predictive current control bandwith 60 Hz at 600W power.

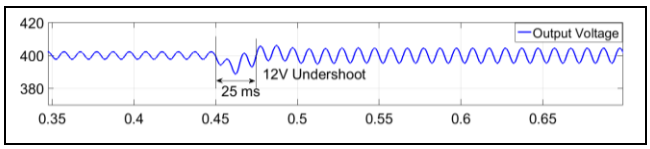

Figure 37. Dynamic response of output voltage during transition from 300W to 600W for predictive current control bandwith 60 Hz.

As shown in Figure 38 and Figure 39, when the output voltage and output power are constant, the output voltage regulation can be achieved at the desired value by determining the K_{max} and K_{min} coefficients at optimal values according to the input voltage value. It is seen that as K_{max} and K_{min} coefficients move away from the optimal values, the output voltage moves away from the desired voltage level.

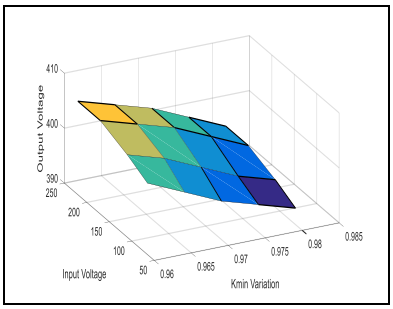

Figure 38. Effect of K_{min} variation on output voltage according to different input voltage.

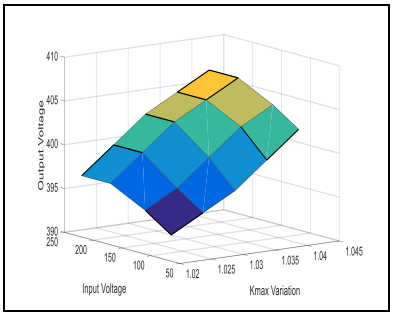

Figure 39. Effect of K_{max} variation on output voltage according to different input voltage.

7 Conclusions

This study shows complete design and modelling of AC/DC True-Bridgeless PFC converter operating in predictive current control with pulse train strategy. When the simulation results are examined, power factors in both of the control methods are close enough to each other to be considered the same. When evaluated in terms of total harmonic distortion, it is observed that harmonic distortion is lower in average current control compared to predictive current control with pulse train strategy. When the system is examined in terms of dynamic response to load changes, it has been observed that since voltage loop and current loop are separated in predictive current control with pulse train strategy, the dynamic response of this method is better than average current control method. Predictive current control with pulse train strategy can be used for power factor correction for bridgeless AC/DC converters. It stands out from other power factor correction methods due to the enhanced dynamic response of the system.

8 Author contribution statement

In this study, Mehmet Fatih Özlük contributed to design and writing of the paper, designing the schematic, the evaluation of the results and review, and Mustafa Gökdağ contributed to the literature review, creating the idea, Ozan Gülbudak contributed spelling and checking of the paper's content and review.

9 Ethics committee approval and conflict of interest statement

“There is no need to obtain permission from the ethics committee for the article prepared”. “There is no conflict of interest between the author and any person or organization contributing to the article”.

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