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Desing of class AB EDDCC+ with the feature of electronic tunability

Elektronik ayarlanabilir AB sınıfı EDDCC+ tasarımı

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Abstract

In this paper, a novel BJT-based class AB electronically tunable plus-type differential difference current conveyor (EDDCC+) is proposed, in which a translinear circuit principle is utilized. The current gain of the proposed EDDCC+ can be easily adjusted externally. Electronically tunability is provided by current sources in the translinear loop. The proposed EDDCC+ is simulated through the SPICE program to indicate the functionality of the proposed EDDCC+, where a previously published KHN filter is used as an application example. AT&T CBIC-R (N-2X and P-2X) transistor model parameters are used in the simulation of this circuit. Simulation results of the KHN filter verify theoretical calculations. The cut-off frequency of the low-pass, high-pass, and band-pass filters in the KHN filter circuit has been electronically changed.

Keywords: Translinear principle, EDDCC+, electronically tunable, BJT, KHN filter.

Öz

Bu makalede, translineer devre prensibinin kullanıldığı yeni bir BJT tabanlı AB sınıfı elektronik olarak ayarlanabilen pozitif tip diferansiyel fark akım taşıyıcı (EDDCC+) önerilmektedir. Önerilen EDDCC+'nın mevcut akım kazancı elektronik olarak ayarlanabilmektedir. Elektronik olarak ayarlama işlemi translineer çevrimde bulunan akım kaynakları ile sağlanmaktadır. EDDCC+'nın işlevselliğini göstermek için daha önce yayınlanmış bir KHN filtresinin uygulama örneği olarak kullanılmıştır. Benzetimler SPICE programı aracılığıyla yapılmıştır. AT&T CBIC-R (N-2X ve P-2X) transistör modeli parametreler önerilen BJT tabanlı EDDCC+'nın benzetiminde kullanılmıştır. Teorik hesaplamalar, KHN süzgecinin benzetim sonuçları ile doğrulanmıştır. Elektronik olarak KHN süzgeç devresinde bulunan alçak geçiren, yüksek geçiren ve bant geçiren süzgeçlerin kesim frekansı değiştirilmiştir.

Anahtar kelimeler: Translineer prensip, EDDCC+, elektronik ayarlanabilirlik, BJT, KHN süzgeç.

1 Introduction

Active building blocks (ABBs) are widely utilized in many analog electronic circuits, such as oscillators, filters, capacitance multipliers, inductor simulators, etc., due to their low power consumption and adjustable properties. The most popular ABBs are current feedback operational amplifiers (CFOAs) [1], operational transconductance amplifiers (OTAs) [2], and current conveyors (CCs) [3]. Many different CCs have emerged from the first designed CCs until today. In this study, differential difference current conveyors (DDCCs) [4] are emphasized due to their input and output relationships.

The controllability of the active elements provides the flexibility of the user and the multiple tasks of the circuit. The translinear principle was introduced by Gilbert in 1975 by making use of the current and voltage relations of the semiconductor elements [5]. According to this principle, forward-biased p-n junctions should form a closed loop, and the number of junctions clockwise should be equal to the number of junctions counterclockwise. In the literature, there are many circuits designed using translinear principles, such as RMS-DC convertors [6], sinusoidal frequency divider circuits [7], logarithmic domain filters [8], [9], and RF RMS detectors [10]. In literature, many circuits with adjustable current gain(s) [11]-[16] have been reported. Nevertheless, effective control ranges of the current gain(s) in [11]-[16] are quite narrow.

In this study, a novel ABB called as an electronically tunable plus-type differential difference current conveyor (EDDCC+) with higher effective control ranges compared to other ABBs [11]-[16] is proposed. The proposed EDDCC+ can be adjusted externally by changing its current gain. The proposed EDDCC+ is simulated via the SPICE program to demonstrate the validity of the proposed EDDCC+ in which a previously published KHN filter [11] is used as an application example.

This paper is organized as follows: the internal structure, terminal equations of the EDDCC+, the current splitter, and current multiplier blocks used in the EDDCC+ are introduced in section 2. In Section 3, a KHN filter that was published in the literature before is treated. Finally, some simulation results and information about targeted future studies are given in Section 4 and Section 5, respectively.

2 Proposed EDDCC+

The equivalent ideal model of the EDDCC+ is shown in Figure 1. It has three resistors and two dependent sources. The values of all three resistors, R_{Y1}, R_{Y2}, and R_{Y3}, are ideally infinity. The relations among the terminals of the EDDCC+ can be defined in Equation (1). The reason for choosing the EDDCC+ is mainly its high mathematical capability, as shown in Equation (1).

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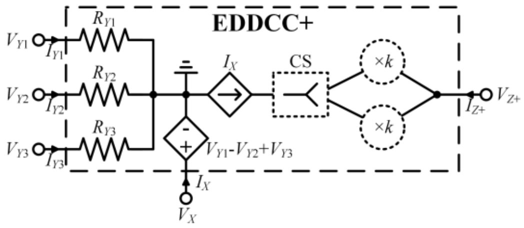

Figure 1. The equivalent model of ideal EDDCC+.

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z+} \\ V_X \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & k \\ 1 & -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \quad (1)$$

In the matrix equation demonstrated above, k is an electronically adjustable current gain. The proposed EDDCC+ has three main parts, as illustrated in Figure 2. The first part consists of BJT-based DDCC [15]. The second part is the current splitter (CS) [17], which is an indispensable element of differential class AB circuits. The last part is the one quad current multiplier (OQM) designed using a translinear principle [18], [19].

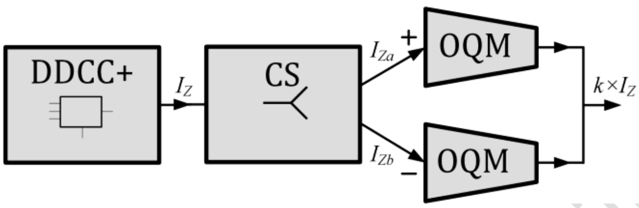

Figure 2. Block of proposed EDDCC+.

CS separates the current, I_Z, into currents, I_{Za} and I_{Zb}; thus, the values of I_{Za} and I_{Zb} are always positive. Thanks to the current splitter, scalar multiplication can be easily realized with single-area multiplication circuits of two positive currents. The relationship among the currents, I_Z, I_{Za}, and I_{Zb} is given below.

$$I_Z = I_{Za} - I_{Zb} \quad (2)$$

The proposed BJT-based internal structure of the EDDCC+ is depicted in Figure 3. The proposed EDDCC+ is a modified version of the commonly used DDCC [4].

On the other hand, the parameters k_1 and k_2 are electronically tunable current multiplier factors. The k parameters can be selected as maximum 3 and minimum 0.05.The values of the k_1 and k_2 are respectively computed as follows:

$$k_1 = \frac{I_7}{I_9} = \frac{I_8}{I_9} \quad (3a)$$

$$k_2 = \frac{I_{10}}{I_{12}} = \frac{I_{11}}{I_{12}} \quad (3b)$$

3 KHN Filter Using the Proposed EDDCC+

KHN filters are one of the well-known circuit types in the literature. KHN filters [11] stand out due to their low element properties, low sensitivity, good stability, etc.

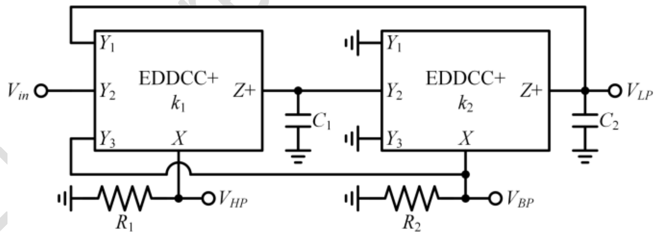

Figure 4. A KHN filter, which is previously published in [10].

If the KHN filter given in Figure 4 is mathematically analyzed, the following high-pass (HP), band-pass (BP), and low-pass (LP) transfer functions are respectively obtained:

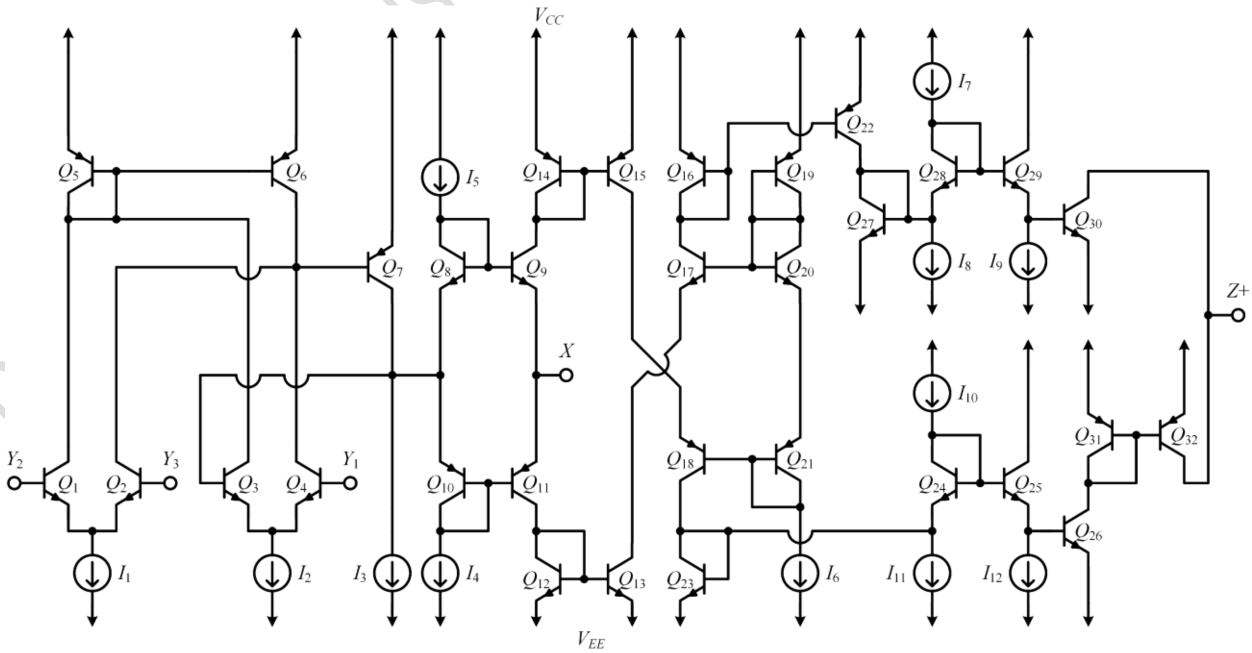

Figure 3. Proposed class AB BJT-based EDDCC+.

$$\frac{V_{HP}}{V_{in}} = \frac{s^2}{s^2 + s\frac{k_1}{R_1C_1} + \frac{k_1k_2}{R_1R_2C_1C_2}} \tag{4a}$$

$$\frac{V_{BP}}{V_{in}} = \frac{s\frac{k_1}{R_1C_1}}{s^2 + s\frac{k_1}{R_1C_1} + \frac{k_1k_2}{R_1R_2C_1C_2}} \tag{4b}$$

$$\frac{V_{LP}}{V_{in}} = \frac{\frac{k_1k_2}{R_1R_2C_1C_2}}{s^2 + s\frac{k_1}{R_1C_1} + \frac{k_1k_2}{R_1R_2C_1C_2}} \tag{4c}$$

The natural frequency and quality factor of the KHN filter given in Figure 4 are respectively shown in Equations (5). As shown in Equations (5), the natural frequency can be electronically adjusted with the parameters k_1 and k_2, without changing the values of the passive elements.

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_1k_2}{R_1R_2C_1C_2}} \tag{5a}$$

$$Q = \sqrt{\frac{k_2R_1C_1}{k_1R_2C_2}} \tag{5b}$$

4 Simulation Results of EDDCC+ and KHN Filter Circuit

The KHN filter is simulated through the SPICE program in which the proposed EDDCC+ structure in Figure 3 is included. The circuit parameters are chosen as follows: $k_1 = k_2 = k$, $V_{CC} = -V_{EE} = 2.5$ V, $R_1=R_2=1$ kΩ, $C_1=C_2=100$ pF, $I_1=I_2=50$ μA, $I_3=100$ μA $I_4=I_5=300$ μA, $I_6=7$ μA, $I_9=I_{12}=40$ μA and $I_7=I_8=I_{10}=I_{11}=k\times40$ μA where AT&T CBIC-R (N-2X and P-2X) BJT parameters given in [18] are utilized. As a result of selecting these values, and BJT paramters, simulation results of the variations of the differantial voltage gain of the EDDCC+ versus frequency is given in Figure 5, while the variations of the current gain versus frequency is indicated in Figure 6.

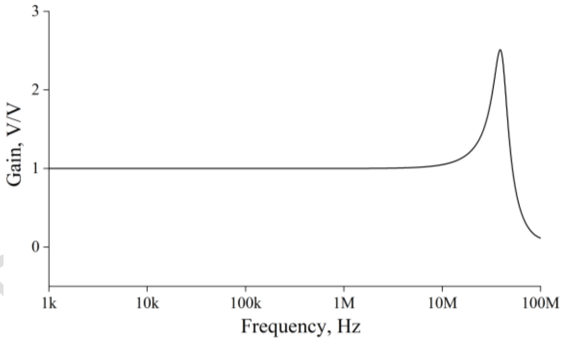

Figure 5. The voltage transfer perfomance of the EDDCC+ versus frequency.

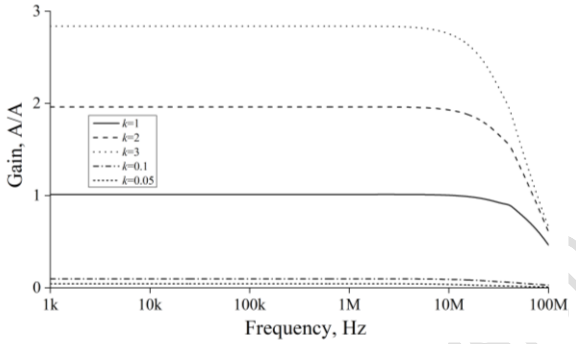

Figure 6. The current transfer with the current gain of the EDDCC+ versus frequency.

For k=1, an AC analysis for the KHN filter demonstrated in Figure 7 is carried out. One observes from Figure 7 that the natural frequency of the KHN filter in Figure 4 is about 1.45 MHz (about 1.59 MHz theoretically) for k=1. If k=0.1 is chosen by selecting $I_7=I_8=I_{10}=I_{11}=4$ μA, and $I_9=I_{12}=40$ μA, the natural frequency of the KHN filter is approximately 145 kHz (about 159 kHz theoretically), which is shown in Figure 8. Similarly, if k=0.05 is chosen by chosing $I_7=I_8=I_{10}=I_{11}=2$ μA, and $I_9=I_{12}=40$ μA, the natural frequency is approximately found as 73 kHz (about 80 kHz theoretically), which is depicted in Figure 9. In Figures 7-9, the simulation results for the HP, BP, and LP outputs of the KHN filter are shown results. The frequency response for different k values of the low-pass filter output of the KHN filter is shown in Figure 10.

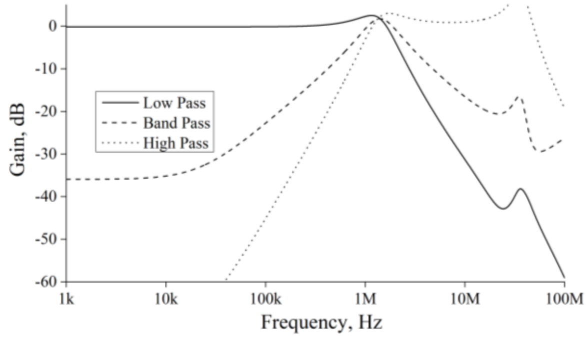

Figure 7. Frequency domain simulation of KHN filter for k=1.

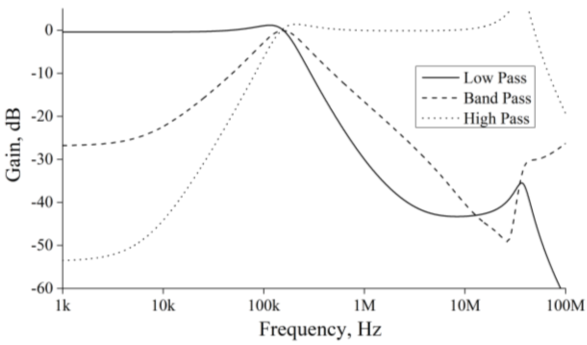

Figure 8. Frequency domain simulation of KHN filter for k=0.1.

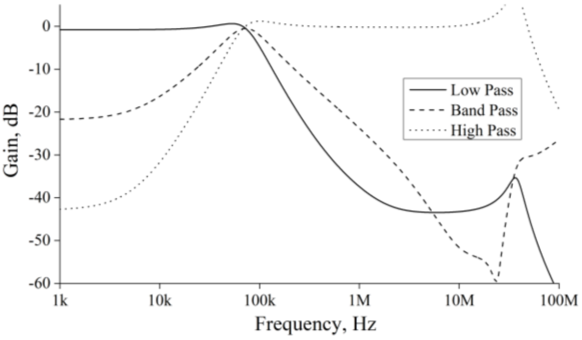

Figure 9. Frequency domain simulation of KHN filter for k=0.05.

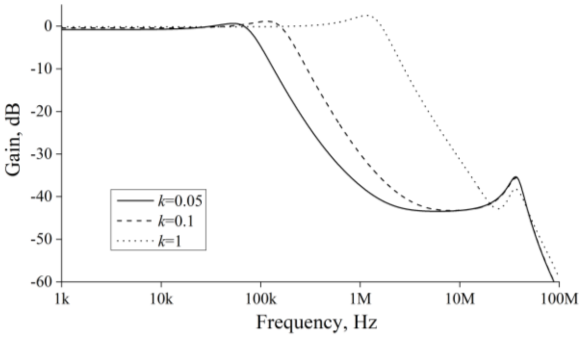

Figure 10. Frequency domain simulation of low-pass filter for different *k* values.

The comparison of various features of the proposed circuit with similar desing in the literature is given in Table 1.

Table 1. Comparison table.

Reference	Number of Transistors	Type of Transistos	Class AB	Multiplier Range
[11]	16	BiCMOS	N.A.	x1-x2
[12]	20	BiCMOS	N.A.	x1-x5
[13]	36	BJT	No	x1-x15
[14]	29	MOS	N.A.	x1-x10
[15]	36	BJT	N.A.	x1-x20
This work	32	BJT	Yes	X0.05-x3

NA:not available

5 Conclusions

In this paper, a novel EDDCC+ is proposed. This novel EDDCC+ is obtained with using CS and OQM connected to the DDCC output; thus, electronically tunable class AB EDDCC+ is achieved. The simulation results of the proposed EDDCC+ show that the proposed EDDCC+ can work up to 1 MHz frequency. To show the workability of the proposed EDDCC+, the previously published KHN filter is simulated via the SPICE program in which the proposed EDDCC+ is used. As can be seen from the simulation results of the KHN filter, the proposed EDDCC+ can also work for different *k* values. Different kinds of circuits, such as tunable oscillators, inductor simulators, etc. can be designed by using the proposed EDDCC+. Future studies aim to improve the performance of EDDCC+ proposed in this paper in various aspects by designing an internal structure with a higher multiplier and working on a different type of transistor-based internal structure. Similarly, it is aimed to design a new analog circuit, such as an analog filter circuit, capacitance multiplier circuit, and inductance simulator circuit that will work in a compatible way with future studies.

6 Author contribution statements

Author 1 in the formation of the idea, the design, simulations and the literature review; Author 2 in the assessment of obtained simulations, results spelling and checking results.

7 Ethics committee approval and conflict of interest statement

There is no need to obtain permission from the ethics committee.

There is no conflict of interest with any person/institution.

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