NEW APPROACHES TO DESIGN DIGITAL PHASE SHIFTERS OVER THE COMPLETE PHASE PLANE

BINBOGA S. YARMAN*

SUMMARY: In this theoretical paper, four different circuit configurations are proposed to design 0°-360° wide range, low loss balanced phase shifters. Each configuration utilizes 3 pin diodes. As a consequence of this work, it is straightforward to construct 180° phase shifting cells for multibit phase array antenna systems using 3 pin diodes. Operation of the new circuits is based upon the phase shifting properties of symmetric low/highpass 3-element LC ladders. Assuming the utilization of lossless pin diodes and ideal reactive element, explicit design equations are presented. A numerical method, which includes the diode losses as well as component parasitic, is also described to design practical phase shifters with minimum balanced loss at a given operating frequency. Examples are included to exhibit the use of explicit design formulas and computer simulations are performed to analyze the loss and phase characteristics of the new circuits. It is expected that new configurations will find application in the commercial and especially military large array antenna systems over the EHF band to be implemented as Microwave Monolithic Integrated Circuits (MMIC).

Key Word: Digital phase shifters.

INTRODUCTION

In the design of large array antenna systems, there is an increasing demand for low loss phase shifters especially at extra high frequencies (EHF). Circuit losses are due to switching elements as well as mismatch and passive components. Device losses, which appear as switching and component losses are inevitable. However, mismatch losses which are due to the choice of circuit topology (such as "intrinsically mismatched loaded lines"), can be omitted by using a proper design concept (1-3).

It has been indicated that mismatch losses are as important as devices losses. Therefore, choice of circuit topology is vital for the realization of low loss, practical phase shifters (3). In our previous work, several circuit configurations for designing 0°-180° digital phase shifters were introduced (3-7). In these configurations, microwave switches, transmission lines and hybrids are not employed. Thus, especially at EHF, losses due to these elements are eliminated.

*From STFA Savronik (Defense Electronics) Co. Tophanelioglu Cad. No. 19, Altunizade, Çamlica, Istanbul, Türkiye.

On the other hand, the phase shifting capability of these circuits is squeezed between 0° to 180° (one half of the phase plane) such that it is not possible to design an exact 180° phase shifting cell using the design concept proposed in references (4-7).

In this paper, four different digital phase shifter configurations are proposed. The circuit structures are similar to those described in (4-7). However, with the new design concept the restricted phase shifting interval of the aforementioned configurations is extended to cover the complete phase plane (0° to 360°). Furthermore when the component losses and parasitic are included among the design parameters, the element values of the suggested circuits are computed in such a way that the insertion loss at each switching state is minimized and balanced at a given frequency f.

Operation of the proposed configurations is based upon the phase shifting properties of the 3-element low/highpass symmetrical ladder networks.

In the new circuits, three pin diodes are employed as switching elements. The diodes are either in back to back

series configuration or in shunt position, either configuration being suitable for monolithic implementation.

For the sake of completeness of the presentation in the following sections, the phase shifting properties of the symmetrical LC ladders and the 0°-180° digital phase shifter" circuits are briefly reviewed. Then, the novel circuit configurations to design "0°-360° wide range digital phase" shifters are presented. A numerical procedure is also described to design minimum loss digital phase shifters in which the diode resistances and the parasitic may be included among the design parameters for practical implementation. Examples are then presented to exhibit the merit of the new circuits.

It is shown that the new circuit configurations yield excellent phase tracking capability up to 20% bandwidth with reasonable loss.

BACKGROUND

It is well known that a 3-element highpass or lowpass symmetric T or π LC ladder can be used as a phase shifting unit at an operating frequency f (8-10). In Figure 1, 3-element LC ladders are shown. As phase shifting cells, the normalized element values of these circuits are given in Table 1 for a specified phase shift θ. The actual values can be obtained by de-normalization with respect to the operating frequency f and the normalization resistance R (in ohms).

In Figure 2, 0°-180° digital phase shifter configurations are depicted. In all the circuit structures, 3 pin diodes are employed as switching elements.

When the diodes are on (forward biased), they ideally act as short circuits and in practice, they can simply be modeled as a small resistance perhaps, is series with some reactive parasites. When the diodes are off (reverse biased), they act as capacitors. In practice however, a series resistance which appears as the diode loss, is associated with the diode capacitor (Figure 3).

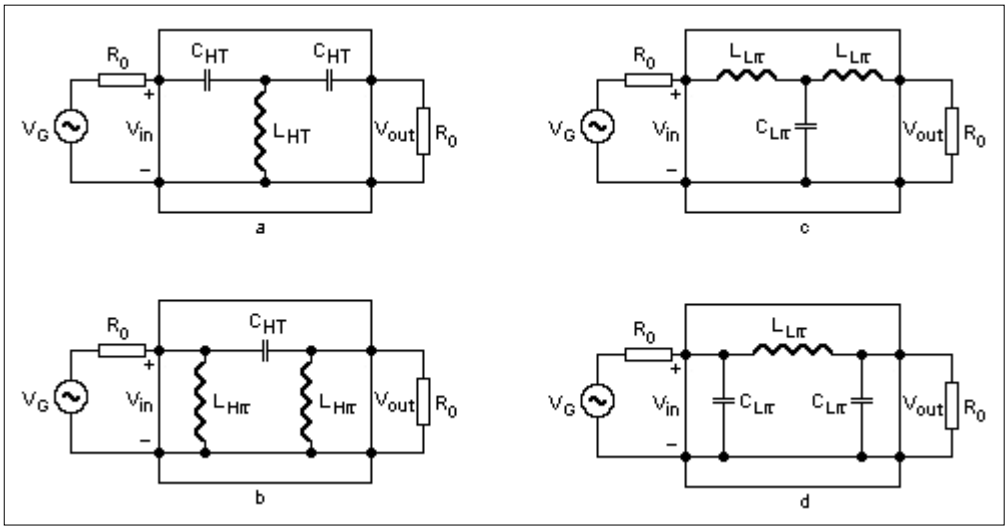
Keeping this operation concept in mind and utilizing Table 1, in one state (say State A) all the configurations shown in Figure 2, act as a low / highpass LC ladder yielding the desired phase shift θ, in the other state (say State B), they act as a piece of parallel pair of wire with no phase shift. Thus the element values of all the 0°-180° digital phase shifters can be derived as shown in Table 2 (3).

0°-360° WIDE RANGE DIGITAL PHASE SHIFTERS

In Figures 4 and 5, T- and π-section based 0°-360° digital phase shifter configurations are introduced. These circuits are similar to those of 0°-180° phase shifters which were described in (3). However, the operation concept is slightly different.

In each of these circuits, the pin diodes are switched on and off, and diode capacitances and the other circuit elements are adjusted in such a way that in one state (say State A), the phase shifter acts as a 3-element lowpass symmetric ladder, yielding the desired phase shift $\theta_A = -(\theta/2)$. In the other state (say State B), it acts as a 3-

Figure 1: Symmetric LC ladders.



a. Highpass-T, b. Highpass-π, c. Lowpass-T, d. Lowpass-π

Table 1: Component values for 3 elemant symmetric LC ladders as phase shifters for a given phase shift θ at the normalizd operating frequency w-1.

HIGHPASS-T	HIGHPASS-π	LOWPASS-T	LOWPASS-π
$\mu = \tan(90°-\theta)$	$\mu = \tan(90°-\theta)$	$\mu = \tan(90°-\theta)$	$\mu = \tan(90°-\theta)$
$C_{HT} = \mu + \sqrt{\mu^2 + 1}$	$L_{H\pi} = \mu + \sqrt{\mu^2 + 1}$	$L_{LT} = \frac{1}{C_{HT}}$	$C_{L\pi} = \frac{1}{L_{H\pi}}$
$L_{HT} = \frac{1 + C_{HT}^2}{2C_{HT}}$	$C_{H\pi} = \frac{1 + L_{H\pi}^2}{2L_{H\pi}}$	$C_{LT} = \frac{1}{L_{HT}}$	$L_{L\pi} = \frac{1}{C_{H\pi}}$

Figure 2: 0°-180° digital phase shifters.

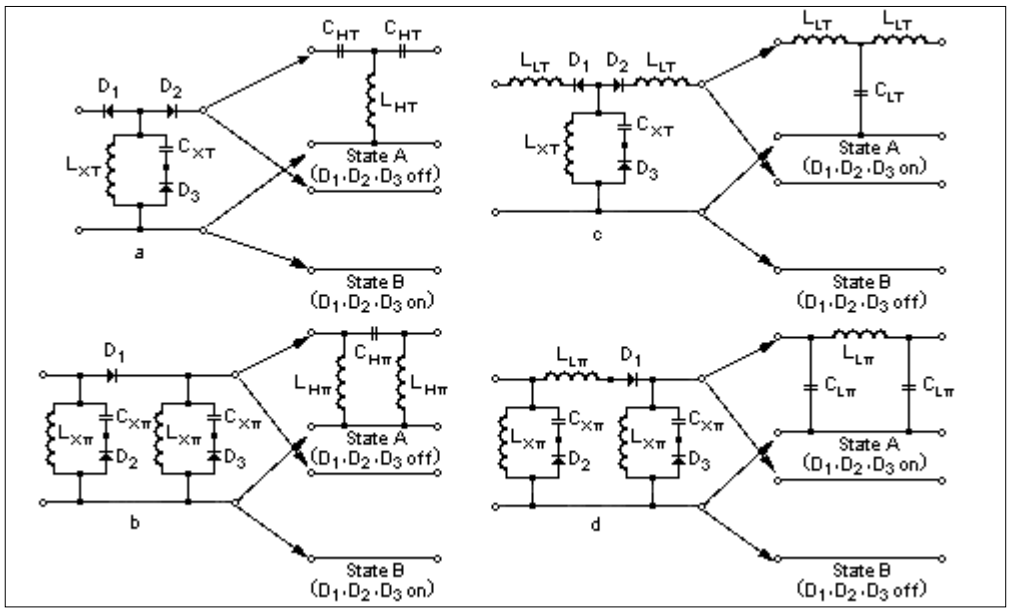
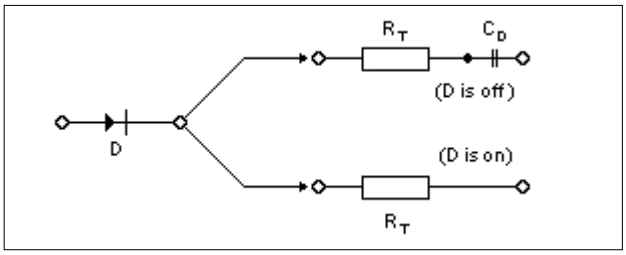


Figure 3: Simple pin diode model.



element highpass symmetric ladder with a desired phase shift $\theta_B = +(\theta/2)$. Thus, at the operating frequency f, the net phase shift between the States B and A is $\theta = \theta_B - \theta_A$.

Since the theoretical phase shifting limits of lowpass and highpass ladders are -(180°) and +(180°) respectively, the complete phase plane (0°-360°) is covered with the operation concept described above. For example, by choosing $\theta/2 = 90°$, an exact 180° phase shift can be obtained with any of these circuits by switching between States A and B.

It is noted that ideally, element values of the proposed phase shifters are computed in such a way that the desired phase shift is achieved with zero loss in each state, at the operating frequency f.

Let us now study the physical operation of the proposed 0°-360° digital phase shifter configurations in detail and derive the explicit design equations.

TYPE I-T SECTION 0°-360° DIGITAL PHASE SHIFTER CONFIGURATION

In Figure 4a, what we call a Type I-T section digital phase shifter configuration is shown. This configuration is exactly the same as the one depicted in Figure 2c, which was previously introduced as the Lowpass Based-T section digital phase shifter. In the present case, the term 'Lowpass Based' has been disregarded, because with the new operation concept, this configuration acts either as a lowpass or a highpass T section depending on the status of the switching diodes.

Consider that in State A, the diodes D_1, D_2 and D_3 are forward biased (ON). In this state, we assume that the circuit performs the operation of a symmetric lowpass T for which the element values are given in column 3 of Table 1, for a specified phase shift $\theta_A = \theta/2$, where θ is the net phase shift between the switching states.

In State B, all the diodes are OFF. In this mode of operation, the circuit acts as a symmetric highpass T. In this case, the element values are listed in column 1 of Table 1 for a desired phase shift $\theta_B = \theta/2$.

Assuming the use of ideal diodes, the normalized element values of Figure 4a are computed at the operating frequency f as follows.

In State A, since the circuit behaves as a symmetric low pass T section, in the series arms the inductance L_L must be equal to L_{LT}, that is,

$$L_L = L_{LT} \tag{1}$$

In the shunt arm, the capacitance C_{LT} is obtained by properly choosing the element values C_X, the diode capacitance C_D and the shunt inductance L_X, that is,

$$C_{LT} = \frac{C_X C_D}{C_X + C_D} - \frac{1}{L_X} \tag{2}$$

when the phase shifter acts as a symmetric highpass T (State B), the equivalent capacitance C_{HT} in the series arm is given by

$$C_{HT} = C_D - \frac{1}{L_L} \tag{3}$$

and in the shunt arm, the equivalent inductance L_{HT} is specified as

$$L_{HT} = \frac{L_X}{C_X L_X - 1} \tag{4}$$

Hence, solving equations (1) - (4) for L_L, L_X, C_D and C_X the explicit design equations are obtained as in Table 3.

TYPE II-T SECTION 0°-360° DIGITAL PHASE SHIFTER

In Figure 4b, a different symmetric T configuration, which is referred to as Type II-T section 0°-360° digital phase shifter is shown. The operation concept of this circuit is similar to that of the Type I-T section configuration.

Here, in State A, the diodes D_1, D_2 are set to be ON and D_3 is OFF. The circuit acts as a symmetric lowpass T with the specified, element values which are listed in Table 1 for the desired phase shift $\theta_A = \theta/2$.

In other words, the following equations are satisfied.

In the series arms,

$$\frac{1}{L_{LT}} = C_A \frac{1}{L_A} \tag{5}$$

in the shunt arm,

$$C_{HT} = \frac{C_D C_X}{C_D + C_X} - \frac{1}{L_X} \tag{6}$$

Similarly, in State B, the diodes D_1, D_2 are OFF and D_3 is ON and the circuit acts a symmetric highpass T. Using the element values listed in Table 1, the equivalent capacitance C_{HT} of the series arm is given by

$$C_{HT} = \frac{C_A C_D}{C_A + C_D} - \frac{1}{L_A} \tag{7}$$

In the shunt arm, the inductance L_{HT} is obtained by properly adjusting the element values C_D , C_X and L_X.

$$-\frac{1}{L_{HT}} = \frac{C_D C_X}{C_D + C_X} - \frac{1}{L_X} \tag{8}$$

Hence, solving the equations (5)-(8) the normalized element values for L_A, L_X, C_A and C_X are found as listed in Table 3.

It should be noted that in this configuration, the designer has the freedom to choose the diode capacitance C_D with the expense of using more elements in the series arms. Depending on design constraints, the circuit may provide technological advantage over the Type I-T structure.

Similar circuits can be constructed as π configurations. In the following sections, these structures are briefly reviewed.

TYPE I-π SECTION 0°-360° DIGITAL PHASE SHIFTER CONFIGURATION

The circuit configuration which is introduced in Figure 5a is named as Type I-π section 0°-360° digital phase shifter. The operation of this circuit is similar to those of

Figure 4a: Type I-T section 0°-360° wide range digital phase shifter.

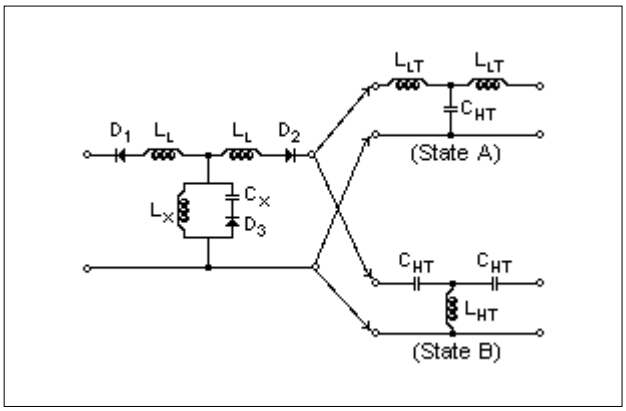


Figure 4b: Type II-T section 0°-360° wide range digital phase shifter.

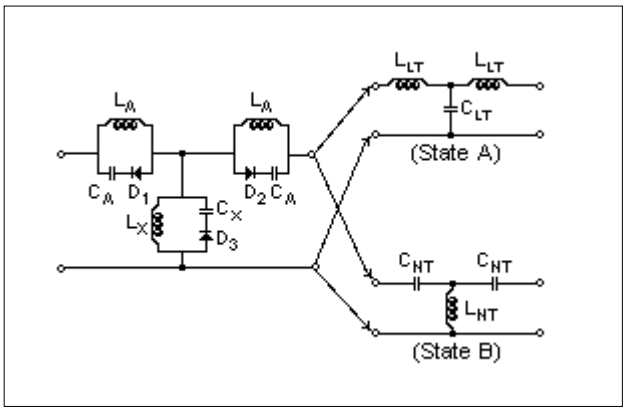


Table 2: Component values for disigning 0°-180° 3 pin diode digital phase shifters.

$F(a,b) = \frac{1+\sqrt{1+4ab}}{2b}$		$f(a,b) = \frac{a+\sqrt{a^2+4ab}}{2}$	
HIGHPASS BASED		LOWPASS BASED	
T-Section	π-Section	T-Section	π-Section
		$L_L = L_{LT}$	$L_L = L_{L\pi}$
$C_D = C_{HT}$	$C_D = C_{H\pi}$	$C_D = C_{HT}$	$C_D = C_{H\pi}$
$a = C_D$	$a = C_D$	$a = C_{LT}$	$a = C_{L\pi}$
$b = L_{HT}$	$b = L_{H\pi}$	$b = C_D$	$b = C_D$
$C_{XT} = F(a, b)$	$C_{X\pi} = F(a, b)$	$C_{XT} = f(a, b)$	$C_{X\pi} = f(a, b)$
$L_{XT} = 1/C_{XT}$	$L_{X\pi} = 1/C_{X\pi}$	$L_{XT} = 1/(C_{XT} - C_{LT})$	$L_{X\pi} = 1/(C_{X\pi} - C_{L\pi})$

Not: Component values are expressed in terms of the two real variable generic functions F (a, b) and f (a, b).

Types I and II-T sections which were described above. In Figure 5a, the switching State A as defined to be the case where all the diodes are ON. In this state, the circuit acts as a symmetric lowpass LC π section of Figure 1d. In State B all the diodes are set to be (OFF) and a highpass π LC ladder operation of Figure 1c is achieved. Employing the element values $L_{L\pi}$, $C_{L\pi}$, $C_{H\pi}$, and $L_{H\pi}$ of Table 1 for the desired phase shifts, which are $\theta_A = -\theta/2$ in State A and $\theta_B = \theta/2$ in State B respectively, the following design equations are obtained.

In State A, the equivalent inductance $L_{L\pi}$ in the series arm

$$L_{L\pi} = L_A \tag{9}$$

In the shunt arms, the equivalent capacitance $C_{L\pi}$ is given by

$$C_{L\pi} = C_X - \frac{1}{L_X} \tag{10}$$

In State B similar equations are written for the highpass π section.

$$C_{H\pi} = C_D - \frac{1}{L_A} \tag{11}$$

$$-\frac{1}{L_{H\pi}} = \frac{C_X C_D}{C_X + C_D} - \frac{1}{L_X} \tag{12}$$

Solving the above equations for L_A, C_A, L_X and C_X, the normalized element values are obtained as listed in Table 4.

TYPE II-π SECTION 0°-360° DIGITAL PHASE SHIFTER CONFIGURATION

In Figure 5b, an alternative circuit structure, the so-called Type II-π section 0°-360° digital phase shifter configuration is presented. Here, the State A operation is defined to be the case, where D_1 is OFF and D_2, D_3 are ON. In this case, the circuit acts as lowpass π LC ladder. In State B, D_1 is forward biased (ON) and D_2, D_3 are reverse biased (OFF). In this mode of operation, the circuit behaves as a symmetric highpass π section. Writing the equivalent impedance equations for States A and B, and solving them for the unknown element values, column 2 of Table 4 is obtained.

As it was the case for Type II-I configuration, here too, the designer has a choice to pick the diode capacitance value C_D. It should be mentioned that using the above operation concept, other circuit configurations may be proposed. Furthermore, the bandwidth of the digital phase shifters may be extended by cascading several sections and optimizing the element values to achieve any desired phase shift θ over the frequency band.

So far, in all the above proposed structures, it has been assumed that the circuit element were ideal. Accordingly, the element values were computed as in Tables 3 and 4. However, this is not the case in practice. For real life problems, one has to consider the diode losses as well as some parasitic in the course of physical implementation. In that case the element values of the proposed phase shifters can not be computed explicitly. Therefore, it may be suitable to formulate the practical design problem as a nonlinear optimization problem. In this case, the ideal element values given in the tables, provide excellent initial estimates for the nonlinear optimization scheme.

In the following section a numerical procedure is suggested to design practical phase shifters into which possible design constraints can easily be imbedded.

A NUMERICAL PROCEDURE TO DESIGN PRACTICAL 0°-360° PHASE SHIFTERS

Let S_{21A} and S_{21B} designate the transfer scattering parameters of the phase shifter circuits in States A and B respectively. Using the polar forms, S_{21A} and S_{21B} can be written on the jw axis.

$$S_{21A}(jw) = r_A(w)\, e^{j\theta A(w)} \tag{13}$$

and

$$S_{21B}(jw) = r_B(w)\, e^{j\theta B(w)} \tag{14}$$

For a given desired phase shift θ and the center frequency f, it is our wish to satisfy the phase shifting conditions. In other words, at the normalized operating frequency w = 1, the amplitude condition,

$$|S_{21A}| = |S_{21B}|$$

or

$$r_A(1) = r_B(1) \tag{15}$$

and the phase condition

$$\theta = |\theta_A - \theta_B| \tag{16}$$

must be satisfied simultaneously. Furthermore, the insertion losses IL_A (w) and IL_B (w) should be minimized in States A and B respectively. That is, at w = 1, let $IL = IL_A(1) = IL_B(1)$ then,

$$IL = 10\log\left[\frac{1}{r_A}\right] = 10\log\left[\frac{1}{r_B}\right] \tag{17}$$

is made minimal.

It should be noted that for the chosen circuit topology r_A, r_B, θ_A and θ_B are the functions of the element values as well as the associated parasitic and losses. For example, in Figure 6, a typical simplified equivalent circuit model is depicted for the Type I-T section 0°-360° digital phase shifter configuration. Here, the diodes are replaced by their equivalents shown in Figure 3 and series resistive losses are affiliated with the ideal inductors. The capacitors are still assumed to be ideal which is valid assumption for many practical cases.

Assuming R_F, R_R and the resistive losses of the inductances are known, one can define an objective function F as follows.

Table 3: Component values for disigning 0°-360° wide range T-section based digital phase shifters.

$\mu = \tan(90° - \theta/2)$	
$C_{HT} = \mu + \sqrt{\mu^2 + 1}$	
$L_{HT} = (1 + C^2_{HT}) / 2C_{HT}$	
$L_{LT} = 1 / C_{HT}$	$C_{LT} = 1 / L_{HT}$
Note: Component values are expressed in terms of two real variables generic functions F (a, b) and f (a, b).	
$F(a, b) = (1 + \sqrt{1 + 2ab}) / b$	$f(a, b) = 2(a + b) / 2ab + b^2$
TYPE I	TYPE II
$C_D = C_{HT} / 2$, $L_L = L_{LT}$	C_D is chosen by the designer
$a = C_D$	$a = C_D$
$b = L_{HT}$	$b = L_{HT}$, $B = L_{LT}$
$C_X = F(a, b)$	$C_X = F(a, b)$, $C_A = F(a, B)$
$L_X = f(a, C_X)$	$L_X = f(a, C_X)$, $L_A = f(a, C_A)$

Figure 5a: Type I-π section 0°-360° wide range digital phase shifter.

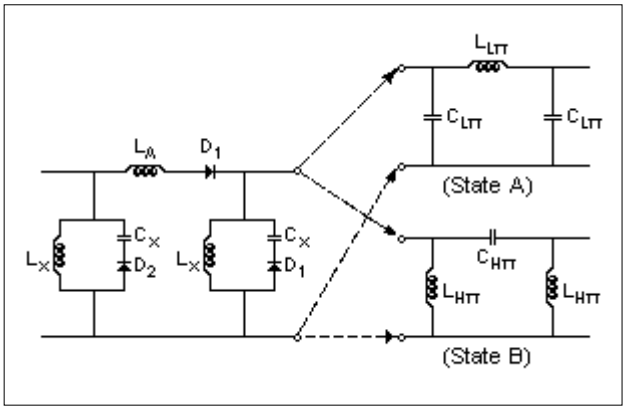
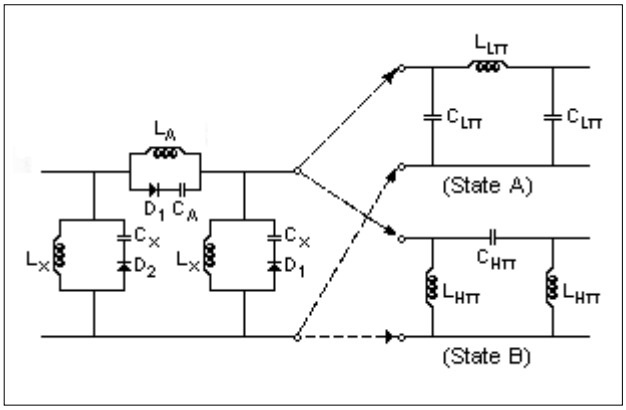


Figure 5b: Type II-π section 0°-360° wide range digital phase shifter.



where S_{21A}, S_{21B}, θ_A and θ_B are expressed in terms of the unknown element values and the fixed circuit parameters such as looses and parasitic. Thus, using a non-linear least-square minimization algorithm (18) is minimized which in turn yields the desired element values. Here it is interesting to note that the 'global minimum' of the objective function F is zero. Therefore, one should avoid to hit local minima during the optimization process.

$$F = \left[|S_{21A}| - |S_{21B}|\right]^2 + \left[\theta - |\theta_A - \theta_B|\right]^2 \qquad (18)$$

Certainly, it is necessary to come up with the initial element values for the phase shifter configuration to run the non-linear minimization program. However, it is natural to start with the ideal element values obtained using the explicit design equations.

It should be noted that in (18), S_{21A} and S_{21B} are forced to be equal to each other at w = 1, but there is no measure imposed to make them minimal at this frequency. The following approach was found very successful to minimize and equalize the insertion losses in the switching states simultaneously.

It is assumed that an unknown variable δ^2 is equal to the sum of the inverse squares of the amplitudes of S_{21A} and S_{21B} at the operating frequency. That is,

$$\delta^2 = |S_{21A}(j^1)|^{-2} + |S_{21B}(j^1)|^{-2} \qquad (19)$$

Then, the new objective function is defined by

$$F = \delta^2 + \left[|S_{21A}| - |S_{21B}|\right]^2 + \left[\theta - |\theta_A - \theta_B|\right]^2 \qquad (20)$$

In the course of minimization of F, while S_{21A} (j^1) and S_{21B} (j^1) are forced to be equal, their amplitudes are also made minimal and the desired phase shift is acquired at the operating frequency.

Since, ideally S_{21A} or S_{21B} is unity, the initial value for the unknown δ^2 is taken to be 2 (or $\delta=\sqrt{2}$).

It is also clear that the above optimization procedure can be carried out over a frequency band if desired. However, in such a case, the phase vs. gain bandwidth trade off should be taken into account.

The numerical method just has been described can be summarized as in the following algorithm.

Figure 6a: A simplified model for the Type I-T section wide range digital phase shifter.

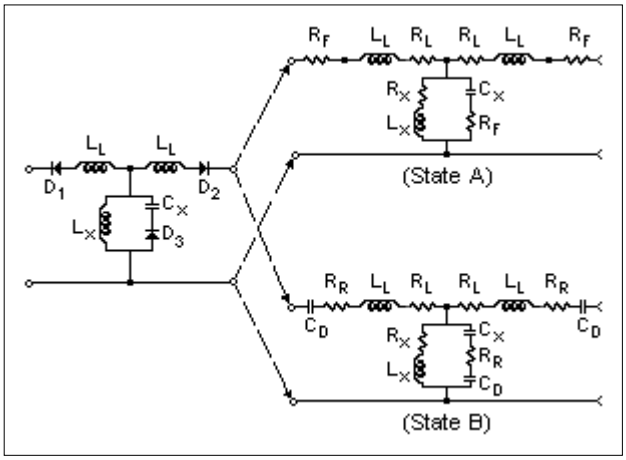


Figure 6b: Ideal phase shifting performance of the 180° digital phase shifter of Type I-T section.

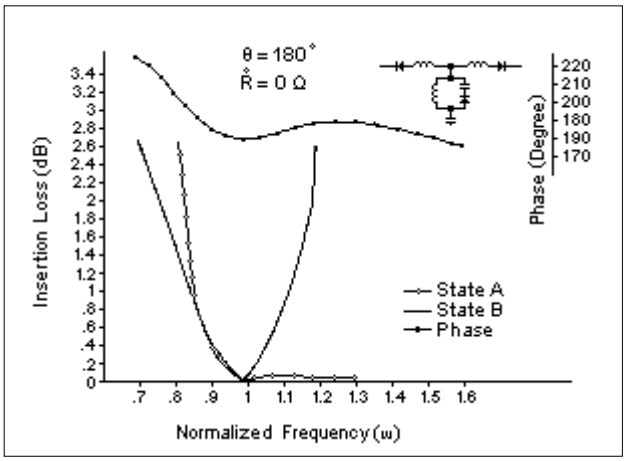


Figure 6c: Lossy phase shifting performance of the 180° digital phase shifter of Type I-T section of example 2.

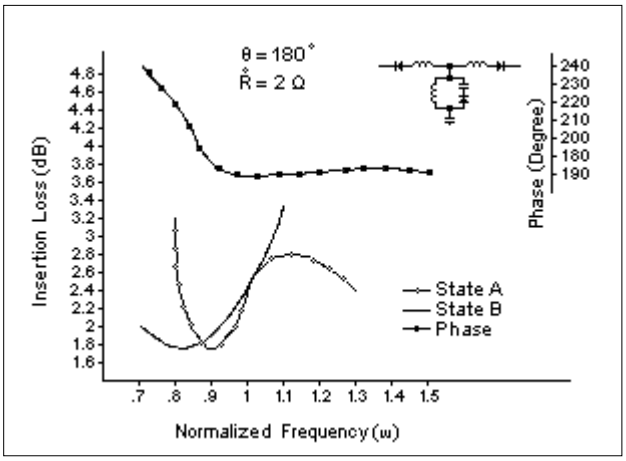


Table 4: Component values for disigning 0°-360° wide range π-section based digital phase shifters.

$\mu = \tan(90° - \theta/2)$	
$C_{L\pi} = (\mu + \sqrt{\mu^2 + 1})^{-1}$	
$L_{L\pi} = 2C_{L\pi} / (1 + C^2_{L\pi})$	
$L_{H\pi} = 1 / C_{L\pi}$	$C_{H\pi} = 1 / L_{L\pi}$
Note: Component values are expressed in terms of two real variables generic functions $F_1(a, b)$, $F_2(a, b)$ and $f(a, b)$.	
$F_1(a, b) = a(1 + \sqrt{1 + 2ab})$	$F_2(a, b) = a + \sqrt{a^2 + 2ab}$
$f(a, b) = 1 / (a - b)$	
TYPE I	TYPE II
$C_D = C_{H\pi} / 2$, $L_A = L_{L\pi}$	C_D is chosen by the designer
$a = C_{L\pi}$	$a = C_{L\pi}$, $A = C_{H\pi}$
$b = C_D$	$b = C_D$
$C_X = F_1(a, b)$	$C_X = F_2(a, b)$, $C_A = F_2(A, b)$
$L_X = f(C_X, a)$	$L_X = f(C_X, a)$, $L_A = f(C_A, A)$

AN ALGORITHM FOR DESIGNING PRACTICAL WIDE RANGE PHASE SHIFTERS

STEP 1: Choose a circuit topology for your phase shifter.

STEP 2: Make a model for your circuit configuration including parasitic and possible losses affiliated with the circuit elements.

STEP 3: Write a computer program which generates the parameters r_A, r_B, θ_A and θ_B in terms of the unknown element values and the known parameters such as losses and parasitic.

STEP 4: In our program, construct the objective function F as given by (20) as a separate subroutine.

STEP 5: Compute the ideal element values using the

formulas given in the Tables to initialize the optimization scheme.

STEP 6: Combine your program which performs the above steps, with and optimization algorithm to minimize the objective function F. The result of the optimization yields the unknown circuit elements.

STEP 7: Having obtained the normalized element values in Step 6, compute the actual values by denormalization.

EXAMPLES

In this section, the usage of the explicit design formulas given in Tables 3 and 4 for designing 0°-360° wide range phase shifter configurations are demonstrated. Then, the practical design algorithm which was presented in the previous section is implemented step by step. In the following examples, $\theta = 180°$ is used as the desired phase shift for the purpose of demonstrations which indicates that wide-range digital phase shifter circuits (including exact 180° cells) can easily be implemented using the new design concept and configurations.

Example 1

In this example, 180° phase shifter cells are designed using the circuit configurations Types I- and II T/π sections. It is assumed that all the circuit elements are ideal. Thus, equations given in Tables 3 and 4 directly apply.

Design of the Type I-T section digital phase shifter: Referring to Figure 4a, the normalized element values of this configuration are computed employing the formulas given in the first column of Table 3. Hence we have,

$$\mu = \tan (90°\text{-}180° / 2) = 0,$$

$$C_{HT} = \mu + \sqrt{\mu^2 + 1} = 1,$$

$$L_{HT} = (1 + C_{HT}^2) / (2C_{HT}) = 1,$$

$$L_{LT} = 1 / C_{HT} = 1,$$

$$C_D = C_{HT} / 2 = 0.5,$$

$$L_L = L_{LT} = 1,$$

$$C_X = F (C_D, L_{HT}) = 2.4142,$$

$$L_X = f (C_D, C_X) = 0.7071$$

Design of the Type II-T section digital phase shifter: In this configuration, the diode capacitance C_D is chosen by the designer. Let $C_D = 1$. Referring to Figure 4b, the normalized element values are given employing the formulas listed in column 2 of Table 3 as follows.

$$C_X = F (C_D, L_{HT}) = F (1, 1) = 2.732$$

$$C_A = F (C_D, L_{LT}) = F (1, 1) = 2.732$$

$$L_{-X} = f (C_D, C_X) = f (1, 2.732) = 0.577$$

$$L_A = f (C_D, C_A) = f (1, 2.732) = 0.577$$

Design of the Type I-π section digital phase shifter: This phase shifter circuit is depicted in Figure 5a and the explicit element values are given in column 1 of Table 4. Following the equations step by step, the subsequent result is obtained.

$$\mu = \tan (90°\text{-}180° / 2) = 0,$$

$$C_{L\pi} = 1 / (\mu + \sqrt{\mu^2 + 1}) = 1,$$

$$L_{L\pi} = 2 C_{L\pi} / (1 + C_{L\pi}^2) = 1,$$

$$L_{H\pi} = 1 / C_{L\pi} = 1, C_{H\pi} = 1 / L_{L\pi} = 1,$$

$$C_D = C_{H\pi} / 2 = 0.5, L_A = L_{L\pi} = 1,$$

$$C_X = F_1 (C_{L\pi}, C_D) = 2.4142,$$

$$L_X = f (C_X, C_{L\pi}) = 0.7071$$

Design of Type II-π section digital phase shifter: As it was the case for Type I-T section design, here too, the diode capacitor C_D is chosen by the designer. Let $C_D = 1$. Then, the element values are given by means of column 2 of Table 4 as follows,

$$C_X = F_2 (C_{L\pi}, C_D) = F_2 (1,1) = 2.732,$$

$$C_A = F_2 (C_{H\pi}, C_D) = F_2 (1,1) = 2.732,$$

$$L_X = f (C_X, C_{L\pi}) = f (2.732, 1) = 0.57735,$$

$$L_A = f (C_A, C_{H\pi}) = 0.57735$$

Example 2

In this example, a practical, Type I-T section digital phase shifting unit of Figure 4a is constructed for the net phase shift $\theta = 180°$. The center frequency f is chosen at 40 Ghz.

It is assumed that the all pin diodes used in this circuit, have identical electrical performances and they all posses the same reverse and forward biased resistances of 1 ohm and have the identical capacitances. It is further presumed that all the inductances included a series 1 ohm resistance and the capacitors are free of loss.

Let us now follow the steps of the practical design algorithm given in the preceding section.

Step 1: Choose the circuit topology: We have already chosen the Type I-T section to Figure 4a.

Step 2: Make a model of the chosen topology: The diodes are represented as shown in Figure 3 with R_F = R_R =1 ohm and a series resistance of 1 ohm is associated with each inductor employed in the circuit. The resulting model is depicted in Figure 6a.

Steps 3 and 4: A computer program was written to generate the equations (19) and (20) also, the objective function F was constructed as described by (21). The unknown parameters of this program are δ, L_A, L_X, C_X and C_D which is the pin diode capacitance to be manufactured as a result of this design.

Step 5: Generation of the initial guess for the optimization: The ideal element values calculated in example 1 for the Type I-T section are used to start the optimization. That is, $\delta=\sqrt{2}$ which defines its ideal value, C_D=5, L_L=1, C_X=2.4142 and L_X=0.7071.

Step 6: Combine your program with an optimization: For this problem, the Levenberg-Marquard algorithm of IMSL package was successfully employed [11, 12]. As a result, the following element values which minimize the objective function were obtained.

L_L= .888897, C_D= .414
C_X= 2.13956, L_X= 1.0064.

The optimization was converged within 12 literation and the minimum of δ^2 was found to be 2.13624.

Step 7: Computation of the actual element values: Using denormalization with respect to 50 ohms and 40 Ghz, the following values are obtained. L_L=0.176nH, C_D=0.0329pF, C_X =0.17pF, L_X = 0.2nH.

The ideal and the lossy performance analysis of this phase shifting cells depicted in Figures 6b and 6c respectively. It is observed that the phase curves are pretty smooth around 180° over the a wide frequency band (about 2 octave) and the insertion loss characteristics in States A and B varies between 0dB and 0.2dB for the ideal design (Figure 6b), and approximately range from 1.8dB to 2.6dB for the lossy design (Figure 6c) over 20% band width. This solution may be considered as a good result at 40 Ghz for a 180° phase shifting unit.

If one wishes to come up with different element values, other circuit topologies can be exercised. For example, the designer has a freedom to choose the diode capacitance value in Type II-T or π sections. Additional tuning capacitors may also be placed in parallel and/or series with the pin diodes to reach to the precise value obtained as the outcome of the optimization.

CONCLUSION

In this theoretical paper, four different digital phase shifter configurations each having the ability of phase shifting between 0° and 360° were presented. The novel circuits include three switching pin diodes which are compact and so are suitable for monolithic implementation. The new circuits have pretty good phase tracking capability over 20% bandwidth as demonstrated by the examples.

Parasitics of the switching diodes, especially can be embedded in Type I-T section structure. Large phase shifts are easily achieved with the new circuits. As opposed to the several design methods, there is no limitation exist to design exact 180° phase shifting cells using the circuits introduced in this work. During the physical implementation, there is no need to utilize ideal microwave switches, loaded lines or hybrids. Therefore, at the Extra High Frequencies (EHF) significant losses due to these elements are eliminated. Hence, it is anticipated that the new circuits are suitable for use at millimeter wave frequencies where the circuit losses are highly critical.

Beyond the explicit equations given for designing ideal phase shifters, a numerical approach was also presented to construct practical phase shifters in which circuit losses and parasitics are easily embedded.

It is expected that the circuit structures and the practical design algorithm described in this paper will find application to design phase array systems at EHF bands both for commercial and military use.

The continuation of this work may be carried out to design WIDE BAND/WIDE PHASE RANGE digital phase shifter by cascading numerous sections. The unknown parameters of the new structures can also be obtained using the numerical method discussed in section ‘A Numerical Procedure to Design Practical 0°-360° Phase Shifters’.

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Correspondence:
Binboga Siddik Yarman
STFA Savronik (Defense Electronics) Co.
Tophanelioglu Cad. No 19,
Altunizade, Çamlica,
Istanbul, TÜRKIYE.